Workshop on
Xilinx 7 Series FPGA's and Vivado Tool flow
22nd January, 2014

Name: Dr/Mr/Ms _____

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Designation: _____

Organization: _____

Address: _____

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Pincode: _____ **Phone:** _____

Mobile: _____

E-Mail: _____

Signature of the Candidate

Important Dates

- **Last date for registration:**20th Jan 2014
- **Program Date:**22nd Jan 2014

Venue:

Department of Electrical Engineering, Indian Institute of Science,
Bangalore, Karnataka -560012

On completion, participants will be able to:

- Describe the key features of Xilinx 7 series FPGA's
- Understand the Vivado design flow
- Develop an embedded system using Zynq
- Address the algorithm to FPGA implementation flow using Vivado HLS
- Understand high-level synthesis flow of Vivado HLS

Course Highlights:

The training program delivers the following key concepts to the participants:

- Architecture and features of 7 series FPGA's from Xilinx
- Xilinx Vivado Tool flow and its comprehensive features overview
- Zynq All Programmable SoC – Architecture
- Embedded Design flow using Zynq
- Vivado High Level Synthesis flow

Department of Electrical Engineering, Indian Institute of Science, Bangalore

The department offers a vibrant environment for postgraduate education and research in Electrical Engineering. Established in 1911, it is one of the first few departments at IISc. The vision of the department is to provide the leadership to enable India's excellence in the field of Electrical Engineering. The department is committed to advancement of the frontiers of knowledge in Electrical Engineering and to provide the students with a stimulating and rewarding learning experience.

The department is currently engaged in research in many areas of Electrical Engineering including Power Systems, Energy Studies, Power Electronics, Electrical Drives, High Voltage engineering, Signal Processing, Image Processing and Multimedia, Biomedical Imaging etc.

The department admits students for 2-year ME programs as well as research programs leading to Ph.D. and M. Sc. (Engg) degrees.

The department is recognized as a Center for Advanced Studies in Electrical Engineering by University Grants Commission.

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CUP strives to drive excellence in teaching-learning experience through setting up world class laboratory infrastructure and enabling the teaching staff and students on the latest tools, technologies and methodologies.

Agenda

This course provides participants an overview of Xilinx 7 series FPGA architecture, Vivado tool flow with emphasis on embedded design flow using Zynq, and Vivado High Level Synthesis concepts.

Objectives

After the completion of this training program the participants will be able to:

- Describe the architecture and features of 7 series FPGA's from Xilinx
- Understand the Vivado design flow
- Understand high-level synthesis flow of Vivado HLS
- Rapidly architect an embedded system targeting the ARM processor of Zynq located on ZedBoard using Vivado and IP Integrator

Pre-requisites:

- Concepts of digital design
- Familiarity with HDL (VHDL or Verilog)
- Digital logic and FPGA design experience
- Basic experience with Xilinx Vivado design software suite
- Basic understanding of C programming
- Basic microprocessor experience

Topics:

- 7-Series Architecture Overview
- Vivado Design Flow
- Lab 1: Vivado Design Flow
  - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bit stream and verify in hardware
- Introduction to Embedded System Design using Zynq
- Lab 2: Simple Hardware Design
  - Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.
- Introduction to High-Level Synthesis using Vivado HLS
- Lab 3**:** Creating Project and Understanding Reports
  - Experience a basic design flow of Vivado HLS and review generated output.

Resource Persons:

- Dr. Parimal Patel, Xilinx University Program
- Mrs. SadiyaArshad, National Manager, CoreEL Technologies
- Mr. Mayur Deshmukh, Applications Engineer, CoreEL Technologies,

Target participants:

- Faculty members
- PG students

Organizing CommitteeConvener:

Sastry P S,
Chairman, Electrical Engineering Department,
Indian Institute of Science

Cost:

This workshop is extended to the participants **free of cost**. Limited seats only; registrations are mandatory.

Address of Correspondence:

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