DC bus imbalance in a three phase four wire grid connected inverter

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Abstract—DC bus imbalance in a split capacitor based rectifier or inverter system is a widely studied issue. In this paper the DC bus imbalance problem has been studied for a three phase four wire grid connected inverter where the midpoint of the split capacitor is connected to the neutral of grid. The problem has been analysed from common mode point of view and subsequently a low frequency common mode model of the entire system has been obtained. The same model helps to find a suitable corrective action. Obtained experimental results confirm the correctness of the theoretical understandings.

Index Terms—DC bus balancing, FEC.

I. INTRODUCTION

A present three phase inverters find wide range of grid connected applications such as Front end converter (FEC) to drives and distributed generating systems, Active filter, Uninterrupted power supply (UPS) etc. IGBT based three phase two level bridge converter has become the standard topology for these applications. In few cases provision for a fourth wire is a necessity. This requirement is met either by a fourth leg in the inverter or by using the midpoint of DC bus capacitors. Generally such requirement arises to cater single phase loads or to provide earth fault protection or in a transformerless application. Here in this paper the problem of DC bus imbalance is addressed for a three phase four wire grid connected inverter where the fourth wire connects the midpoint of DC bus capacitors to the neutral point of grid. DC bus imbalance in a split capacitor converter is a widely studied issue [1]–[4]. Generally two precision resistors are used to divide the bus voltage equally between the two capacitor. But because of offset present in the sensed current and voltages, the neutral or the wire connected to the midpoint of DC bus capacitor carries a ‘DC’ current which causes one of the bus voltage to rise and the other to decrease resulting in DC bus imbalance [1]–[5]. Finally one of the bus voltage gets clamped to the peak of phase voltage. Present literatures show that the corrective action can be taken in two ways. First one is by adding a feed-forward or compensating term to the modulating signal [3]–[5] to inject a ‘DC’ current into the system and the second one is by generating a current reference which is to be tracked by the current controller such that the voltage imbalance is forced to zero [2], [5]. Here in this work a low frequency common mode model of the entire system has been developed to understand the imbalance issue. The similarity of this analysis with the existing approach has been pointed out. Further the same common mode model has been used to derive a suitable controller to mitigate the problem.

II. DC BUS IMBALANCE PROBLEM

The structure of a 3 phase 4 wire LCL filter based grid connected inverter is shown in Fig. 1. The midpoint of the DC bus is connected to the neutral point of the grid. The problem to be looked into here is unequal voltage distribution in the DC bus or voltage imbalance between top (PO) and bottom (ON) DC bus. The resistance \( R_d \) in the DC bus side are the voltage balancing resistors. Here \( R_d = 25 \text{ k}\Omega, 25 \text{ Watt} \). DC bus capacitances, \( C_d \), are of 3300 \( \mu F, 500 \text{ V} \). The requirement here is to keep the total bus voltage at a specified voltage \( V_{dc} \) (1) and the difference between top (PO) and bottom (ON) DC bus voltage, \( \Delta v \), should be ‘zero’ (2). Under these conditions the bus voltage would be equally distributed in the two capacitors (3).

\[
\begin{align*}
\Delta v &= v_{PO} - v_{ON} = 0 \\
v_{PO} &= v_{NO} = \frac{V_{dc}}{2}
\end{align*}
\]

The voltage imbalance problem is generally analysed by using KCL at the DC bus side. The same dynamic equation can easily be achieved by doing a common mode analysis.
III. MODELLING OF AC SIDE

If duty ratio at any instant is \( d_i \), then average pole voltage on AC side can be written as shown in (9).

\[
v_i = d_i \, v_{PO} - (1 - d_i) \, v_{ON} \quad \text{Here } i = R, Y, B
\]

\[
\Rightarrow \quad v_i = d_i (v_{PO} + v_{ON}) - v_{ON}
\]  (9)

From (1) and (2) \( v_{PO} \) and \( v_{ON} \) can be written as

\[
v_{PO} = \frac{v_{dc} + \Delta v}{2}
\]

\[
v_{ON} = \frac{v_{dc} - \Delta v}{2}
\]  (10)

Now for sine triangle PWM technique duty ratio \( d_i \) is related to modulating signal \( m_i \) by (11).

\[
d_i = 0.5 + 0.5 \, m_i
\]  (11)

Again, \( m_i \) can be composed of a DC part and an AC part

\[
i.e. m_i = m_{dc} + m_{ac}.
\]

Therefore using this relationship along with (9), (10), and (11), average pole voltage can be expressed as shown in (12).

\[
v_i = m_{dc} \, v_{dc}^2 + \frac{\Delta v}{2} + m_{ac} \, v_{dc}^2
\]

\[
\Rightarrow \quad v_i = (m_{dc} \, v_{dc}^2 + v_{com1}) + m_{ac} \, v_{dc}^2
\]  (12)

Common mode voltage at the terminals of inverter which is average of the three pole voltages can be expressed by (13). Further simplification shows that common mode voltage at the AC terminals of inverter can be represented by (14).

\[
v_{com2} = \frac{v_{RO} + v_{YO} + v_{BO}}{3} = \frac{1}{3} \sum v_i
\]  (13)

\[
\Rightarrow \quad v_{com2} = m_{dc} \, \frac{v_{dc}}{2} + v_{com1}
\]  (14)

Here the assumption is that the injected DC offset in all phases are equal. The low frequency common mode model of inverter at the AC terminal is represented by (14). The equivalent circuit is shown in Fig. 3.
IV. LOW FREQUENCY EQUIVALENT MODEL AND IMBALANCE MITIGATION

The AC terminals, R,Y and B (Fig. 1), are at same potential from common mode point of view. Hence the 3 phases of LCL filter can be reduced to a single equivalent circuit. Combining this with low frequency common mode equivalent circuit of inverter, an equivalent circuit for the entire system can be obtained. Fig. 4 represents the low frequency common mode equivalent circuit of the total system. From this equivalent circuit it becomes clear that the ‘DC’ current flowing in neutral wire can be controlled by regulating ‘$m_{dc}$’ to achieve $v_{com1} = 0$. This will ensure that the DC bus voltage is equally distributed in the two capacitors. Following section discusses the design of a suitable controller to mitigate DC bus imbalance problem.

V. CONTROLLER DESIGN

Let us assume that the 3 phase 4 wire inverter with LCL filter is being used as a DSTATCOM. The main control strategy with the DC bus imbalance correction is shown in Fig. 5. Here in this paper controller design part for the imbalance correction is discussed. The objective here is to make $v_{com1} = \frac{\Delta v}{2} = 0$. So the reference value for difference between two capacitor voltages is set at $\Delta v^* = 0$. As the two DC bus voltages are sensed so $\Delta v$ can be calculated easily. The error between the reference and the measured value is passed through a PI controller to obtain the compensating current reference. The current controller used here for controlling the fundamental current is a PR controller. This will act as a proportional controller for this compensating current reference which is DC in nature. The closed loop control block diagram is shown in Fig. 6.

VI. EXPERIMENTAL RESULT

During experiment initially each half of DC bus was pre-charged closed to a voltage of 100 V. Then a command was initiated to boost it to a total of 300 V. Without corrective action the DC bus settled with a $\Delta v = 30 V$, as seen in Fig. 7a. When the corrective action was activated the voltages were brought to 150 V as set by the reference (Fig. 7b). Fig. 7c shows the charging of DC bus to the reference of 300 V with the corrective action.

VII. CONCLUSION

In this paper the DC bus imbalance problem present in a 3 phase 4 wire grid connected inverter has been investigated. The problem has been analysed by making
Fig. 5. Total system diagram along with control blocks

Fig. 6. Closed loop control block diagram for DC bus imbalance correction
a low frequency common mode equivalent circuit of the entire system. A suitable controller has been designed to mitigate the problem. The experimental results obtained confirms the theoretical understandings.

REFERENCES


