Load Test on High Current Low Voltage Inverters in Back-to-Back Connection

A Project Report
Submitted in Partial Fulfilment of
Requirement for the Degree of
Master of Engineering
in
Electrical Engineering

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June 2011
Acknowledgements

I am grateful to Prof V.T.Ranganathan, for offering me this exciting project. I sincerely thank him for his patience and motivation. In the name of Electric Drives course, he covered almost everything.

I sincerely thank Dr. Vinod John for his valuable suggestions and guidance given right from the hardware design to till the end of the project. His consistent guidance motivated me a lot.

I would like to thank Prof. G. Narayanan for his courses and the challenging assignments right from Electronics Circuits lab to PWM course.

I thank Dr. Udaya kumar and Dr. M.K. Gunasekaran for their exceptional lectures.

I specially thank Arun KaruppaSwamy, Senthilkumar(NITT), Shankar, Sujata, Abhijit, Anirban, Anil, Prashant for their suggestions and help during the project. I also thank Leela krishna, Ibrahim, Srikanth, Chandramouli, Francis, Deba for all the non-technical engagements that we had.

I thank Mr. H.N. Purushothama, Mr. K. Jagannath Kini, Mr. D.M. Channegowda, Mr. B.K. Chandrashekar, at the department office for their good and kind administrative activities.

I thank Ms. Silvi Jose, Mr. Ravi, Mr. Paul, and members of the department workshop for their help during the project.
Abstract

High Current Low Voltage Inverters are generally used in automotive applications. Performing direct load test on these inverters results in lot of power loss. Generally Regenerative Load Tests are preferred over direct load tests. The Obvious reasons are efficient way of testing and more loss calculation accuracy. It can be tested for any load condition. But this method requires two identical power converters.

![Inverter - Regenerative Load Test](image)

**Figure 0.1: Inverter - Regenerative Load Test**

**Basic Concept:** When one converter makes DC-to-AC as Inverter and the other operating as a rectifier, put back the power in to the DC source again. Ultimately the power drawn from the DC source is only for the losses of both the inverters.

To test the inverters at various active and reactive load conditions, initially simulation has been done with closed loop control using SIMULINK. Then the Hardware Setup has been built and the control has been implemented using TMS320F2812 processor. Regenerative test has been done at various power levels and the losses are plotted.
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Chapter 1

Introduction

The load test setup is shown in fig.1.1. The DC sides of both the inverters are connected together, while the inverter output terminals are connected through the inductors. By modulating the legs appropriately, the voltage across the inductor can be defined. This defined-voltage defines the current in the inductor.

![Figure 1.1: Back-to-back setup](image)

When the inverters are under sinusoidal modulation, assume \( V_g \) is the voltage of inverter-1 and \( V_i \) is the voltage of inverter-2. Now the voltage the inductor is vector difference of \( V_g \) and \( V_i \). Fig.1.2 shows the various active and reactive flow conditions.

By controlling the magnitude and phase angle of the inverter voltages, we can drive the current through inverters for various operating conditions.
Chapter 1. Introduction

Vg and Il are in-phase

Inv-2 acts as a pure resistive load

Current flowing in opposite

Inv-2 sees a pure resistive load

Inv-2 acts as a pure capacitive load

Inv-2 acts as a pure inductive load

Figure 1.2: Power flow at various power factors

1.1 Organization of the thesis

Chapter 2 deals with modeling of the system in rotating axis reference frame and the design of appropriate PI-controller for closed loop control.

Chapter 3 Hardware Design - explains, design of the inductor including the thermal effect, capacitor selection and MOSFET loss calculation and also describes the design of current and voltage sensors and shows the changes made in the present Protection and Delay Card

Chapter 4 Simulation Setup and the Digital Implementation of the control section in the hardware

Chapter 5 shows the results from simulation as well as from the experimental setup and the conclusion is given in chapter 6
Chapter 2

System Modeling and Controller Design

2.1 3 phase System Modeling

Now the aim is to control the inductor current $I_L$, by controlling the voltage sources across which the inductor is connected. It seems we need to control the six voltages, of six legs totally. But the control thing can be made much more simple, by operating one inverter at a fixed operating voltage. In this case, the second inverter which carries the $V_i$ notation is assumed to be operating at constant voltage. i.e., The 2nd inverter is modulated by a constant sine-triangle modulation.

So the control of 1st inverter alone serves the purpose. As depicted in the fig.1.2, by making $V_g$ to lead or lag the $V_i$, we can make the inverter1 to see an active AC load connected.
To include the reactive part, we need to make the $V_g$-magnitude different from the magnitude of $V_i$ (bottom diagrams of fig.1.2)

The system equations are,

\[ V_{g1} = L \frac{di_{L1}}{dt} + i_{L1}R + V_{i1} \quad (2.1) \]
\[ V_{g2} = L \frac{di_{L2}}{dt} + i_{L2}R + V_{i2} \quad (2.2) \]
\[ V_{g3} = L \frac{di_{L3}}{dt} + i_{L3}R + V_{i3} \quad (2.3) \]

R - internal resistance of the inductor.

2.2 Modeling in Rotating Reference Frame

2.2.1 System Equation in 2phase quantities

To make the conversion process simpler, initially the system equations are converted to 2-phase quantities. In this conversion, zero sequence also included. The necessity of zero sequence is discussed in section 2.4.

\[ V_{ga} = L \frac{di_{La}}{dt} + i_{La}R + V_{ia} \quad (2.4) \]
\[ V_{gb} = L \frac{di_{Lb}}{dt} + i_{Lb}R + V_{ib} \quad (2.5) \]
\[ V_{g0} = L \frac{di_{L0}}{dt} + i_{L0}R + V_{i0} \quad (2.6) \]

2.2.2 System Equation in Rotating Reference

The zero sequence component is perpendicular to the rotating vector. So, we do not need to consider it for the conversion of static to rotating reference frame. So combining the equations 2.4 and 2.5,

\[ V_{ga} + jV_{gb} = L \frac{d(i_{La} + ji_{Lb})}{dt} + (i_{La} + ji_{Lb})R + (V_{ia} + jV_{ib}) \quad (2.7) \]

The conversion equation for ab-dq axis system,

\[ (V_a + jV_b) = (V_d + jV_q)e^{j\theta} \quad (2.8) \]
\[ \frac{d\theta}{dt} = \omega \quad (2.9) \]
Substitute eq.2.8 and eq.2.9 in eq.2.7, and separate Real and Imaginary parts

\[
V_{gd} = L \frac{di_d}{dt} + i_d R + V_{id} - \omega Li_q \tag{2.10}
\]

\[
V_{gq} = L \frac{di_q}{dt} + i_q R + V_{iq} + \omega Li_d \tag{2.11}
\]

The rotating voltage vector \(V_i\) of the 2\textsuperscript{nd} inverter is assumed to be aligned with \(V_{iq}\). Therefore, the final system equations in the rotating axis reference frame is,

\[
V_{gd} = L \frac{di_d}{dt} + i_d R - \omega Li_q \tag{2.12}
\]

\[
V_{gq} = L \frac{di_q}{dt} + i_q R + V_{iq} + \omega Li_d \tag{2.13}
\]

The s-domain system equations are,

\[
V_{gd} = s Li_d + i_d R - \omega Li_q \tag{2.14}
\]

\[
V_{gq} = s Li_q + i_q R + V_{iq} + \omega Li_d \tag{2.15}
\]

Figure 2.2: Control Block representation of the System in dq

### 2.3 Controller Design

#### 2.3.1 Feed Forward

Controller can be designed only for the linear systems. To make the system linear, we need to add the feed forward terms in the controller section. So that the PI controller sees the system as linear. The closed loop control including the feed forward terms has been shown in the fig.2.3

#### 2.3.2 Feedback Filter design

Feedback Filter is used to eliminate the current ripple because of switching component. Inverter is operating at the switching frequency of 20kHz. This component has to be filtered
2.3.3 PI controller design

Time constant of the PI controller is chosen to be equal to the system time constant ($T_c = \frac{sL}{R}$). Therefore the system pole cancels with PI controller zero. Fig. 2.4 shows the minimized system representation after pole-zero cancellation.

Still, reduce the above system, we end up with a second-order equation. For the damping ratio of 1,

$$K_c = \frac{R_a T_c}{K_f G T_f}$$  \hspace{1cm} (2.16)
2.4 Necessity of Zero Sequence Control

Generally the most of the three-phase systems are not neutral point connected. So slight unbalances in the system will not cause any problem to the system or the control. But this system is Neutral connected system as shown in fig.2.5

Small unbalance in the system may cause, a resultant presence of a average DC voltage. This DC voltage is infinitely integrated by the inductor and it can cause saturation problem. So it is safer to include the zero sequence controller along with d and q axis current controllers.
Chapter 2. System Modeling and Controller Design

2.5 Reference Frame Conversion

2.5.1 Static to Rotating Frame conversion

3phase to 2phase conversion:

\[ V_a = V_1 - \frac{V_2}{2} - \frac{V_3}{2} \]  
\[ V_b = \frac{\sqrt{3}}{2} V_2 - \frac{\sqrt{3}}{2} V_3 \]  
\[ V_0 = \frac{V_1}{3} + \frac{V_2}{3} + \frac{V_3}{3} \]  

2phase to Rotating Frame conversion:

\[ V_d = V_a \cos \theta + V_b \sin \theta \]  
\[ V_q = -V_a \sin \theta + V_b \cos \theta \]  
\[ V_0 = V_0 \]  

2.5.2 Rotating to Static Frame conversion

Rotating to 2phase Frame conversion:

\[ V_a = V_d \cos \theta - V_q \sin \theta \]  
\[ V_b = V_d \sin \theta + V_q \cos \theta \]  
\[ V_0 = V_0 \]  

2phase to 3phase conversion:

\[ V_1 = \frac{2}{3} V_a + V_0 \]  
\[ V_2 = -\frac{1}{3} V_a + \frac{1}{\sqrt{3}} V_b + V_0 \]  
\[ V_3 = -\frac{1}{3} V_a - \frac{1}{\sqrt{3}} V_b + V_0 \]  

All the values are instantaneous.

123 - 3 phase Static reference frame
ab0 - 2 phase Static reference frame
dq0 - Rotating reference frame
Chapter 3

Hardware Design

The Hardware design of the entire power setup is being explained in this chapter. The DC voltage $V_{dc}$ of the system is 48V and the RMS inductor current is 50A. This chapter explains,

- High-current inductor design
- Choosing the Switching device and loss calculation
- DC bus capacitor selection

3.1 Inductor Design

3.1.1 Inductance value

The DC bus voltage is 48V. The maximum value of sinusoidal voltage obtainable from a leg is 24V. Since there is limit in the minimum pulselength for any switching device, it has been decided to fix the maximum duty ratio as 0.866.

Therefore maximum AC voltage obtainable = $0.866 \times 24 = 20.78V$.

The $RMS_{max}$ value is = 14.7 V

14.7V is the maximum RMS AC voltage obtainable from any leg of the inverter. We need to have voltage difference between the inductor for the current flow. As per general convention, 10% drop across the inductance is allowed.

The 10% of 14.7 V is 1.47. The maximum AC RMS voltage drop across the inductance is 1.47V. The maximum AC RMS current through the inductor is 50A. Therefore

$$X_L = \frac{1.47}{50} = j29.4m\Omega \quad Inductance L = \frac{X_L}{2\pi f} = 94\mu H$$
Since the idea is to build 2-separate inverter setups, it has been decided to build six inductors of 48\(\mu\)H as shown in the fig.3.1

![Diagram of inverter setups](image)

**Figure 3.1: Series connected 48\(\mu\)H Inductors**

### 3.1.2 Inductance Parameters

#### 3.1.2.1 Core Selection

Since the inductance is designed to operate in high current, it is wiser to choose a core with higher saturation flux density \((B_{\text{max}})\). It will reduce the size of the inductance. Amorphous core is chosen, it has \(B_{\text{max}}\) of 1.5T.

Based on the \(A_L\) value of the core, number of turns has been calculated.

\[
N = \sqrt{\frac{L}{A_L}} \quad (3.1)
\]

where \(N\) is the number of turns of copper winding and \(L\) is the required inductance. The unit of \(A_L\) here is \(\mu\)H/\(\text{turns}^2\).

\textit{AMCC-40} core has been chosen with an air-gap of 1.5mm and \(A_L\) value of 0.273. Therefore for an inductance value of 48\(\mu\)H, number of turns,

\[
N = \sqrt{\frac{48}{0.273}} = 13\text{ turns}
\]

It has been made sure that \(A_L\) is almost constant till the maximum value of Magnetizing force (ampere-turns) Fig.3.2
### 3.1. Inductor Design

\[ N \times I_{pk} = 13 \times 71 = 923 \text{ ampere-turns} \]

![AMCC-40 Inductance Curves](image)

Figure 3.2: \( A_L \) vs \( H \) for AMCC 40 core. Source: Metglas Inc[2]

Maximum flux density (\( B_m \)) is calculated and it has been verified that it is not crossing the limit.

\[
B_m = \frac{A_L N I_{pk}}{A_e} = \frac{0.273 \times 10^{-6} \times 13 \times 71}{3.7 \times 10^{-4}} = 0.681T
\]  

(3.2)

#### 3.1.2.2 Copper selection

Since it is a high current (50A), low frequency (50Hz) and low voltage (48V) application, the inductance reactance is very less (30m\(\Omega\)). The conductor resistance should also be very less to meet the electrical requirement (high \( X_L / R \) ratio) and thermal requirement (less power loss).

For 50A current, required cross section area of the conductor

\[
A = \frac{I_{rms}}{J} = \frac{50}{3.5} = 14.2857 \text{mm}^2
\]

where \( J \) - current density (assumed as 3.5A/mm\(^2\)).
Chapter 3. Hardware Design

Since the cross-section area is more, it has been decided to use four conductors in parallel. The required diameter of the conductor,

\[ d = \sqrt{\frac{A}{\pi}} = \sqrt{\frac{14.2857}{3.5}} = 2.1324\text{mm} \]

where \( A = 4 \times \frac{\pi \times d^2}{4} \)

For this diameter, 13-SWG wire is chosen (which has diameter of 2.337mm).

3.1.2.3 Resistance Calculation

The approximate mean length of one turn is \( (2 \times (35 + 6 + 6) + 2 \times (13 + 6 + 6)) = 144\text{mm} \)

Therefore for 15 turns, the total length is \( 13 \times 144 = 1.872\text{m} \).

Total cross section \( A = 4 \times \frac{\pi \times d^2}{4} = 4 \times \frac{\pi \times 2.337^2}{4} = 17.158\text{mm}^2 \)

Resistance at \( 20^\circ C \)

\[ R = \frac{\rho l}{a} = \frac{1.725 \times 10^{-8} \times 1.872}{17.158 \times 10^{-6}} = 1.882\text{m}\Omega \]

Resistance at \( 90^\circ C \)

\[ R = R_0[1 + \alpha(T - T_0)] = 1.87m\Omega[1 + 3.9 \times 10^{-3} \times (90 - 20)] = 2.4\text{m}\Omega \]

where \( \alpha \) is Temperature co-efficient of Copper

3.1.3 Power Loss

3.1.3.1 Harmonic Spectrum of Inductor Voltage

To study the losses in the inductor, the legs are assumed to be modulated by Sine-Sawtooth modulation at 10kHz of carrier frequency. The Frequency Spectrum of voltage across the inductor has been calculated. fig.3.3

The loss component can be split into two components. One is core loss and the other is Copper loss.
3.1. Inductor Design

3.1.3.2 Core Loss

The total core loss (including Hysteresis and Eddy current losses) per kg,

\[ P_{\text{core}} = \sum 6.5f_n (kHz)^{1.51} B_n(T)^{1.74} W/kg \]  

(3.3)

where \( B \) - Flux Density (Maximum AC value) , \( n \)-th harmonic

\( B_n \) - for each frequency can be calculated from the voltage spectrum.

\[ B_n = \frac{L I_{pk}}{NA_c} \]  

(3.4)

\[ I_{pk} = \frac{V_n}{2\pi f L} \]  

(3.5)

Core loss,

\[ P_{\text{core}} = \sum 6.5 \times \left( \frac{f_n}{1000} \right)^{1.51} \times \left( \frac{V_n}{2\pi f NA_c} \right)^{1.74} = 0.2871 W/kg \]  

(3.6)

Weight of the AMCC40 core = 0.53 kg

The Total Core loss \( P_{\text{core}} = 0.2871 \times 0.53 = 0.1522 \) W
3.1.3.3 Copper Loss

The resistance of the winding varies with the frequency, because of skin effect and Proximity effect. For a round conductor, at 50Hz we can neglect the skin effect. From the frequency spectrum(fig.3.3), the harmonic components are around the 10kHz and its multiples.

At these frequencies, because of Proximity and Skin effects the resistance increases by many folds. To calculate the resistance accurately at these frequencies, we need to solve Bessel functions. Since the presence of harmonics is at high frequency compared to the fundamental, the reactance offered by the inductance is very high and we can all most ignore it. Extreme case analysis can be done, to determine the effect of harmonics in copper loss calculation.

In any RL circuit, the maximum power dissipated in the resistance is maximum, when the reactance of the inductor is equal to the resistance.

\[ R = X_L = 2\pi f L \]

It has been assumed that the resistance for each harmonic component (except for the fundamental) is equal to the reactance and the power loss calculation has been done.

\[ P_{Cu} = 50^2 \times 2.4m\Omega + \sum \left( \frac{V_n}{2\pi nfL + j \times 2\pi nfL} \right)^2 \times 2\pi nfL \]

\[ = 6 + 0.98 = 6.98 \text{ W} \]

where \( 2 \leq n \geq \infty \)

For calculation, till 2000\textsuperscript{th} harmonic has been taken into account. Even at the extreme case, the power loss because of harmonics is only one watt, while the copper loss of fundamental component is 6W. So, there is no harm in assuming the total copper loss as 7W.
3.1.3.4 Total loss

\[ P_{loss} = P_{Cu} + P_{core} = 6.98 + 0.1522 = 7.1322 \text{ W} \]

3.1.4 Thermal Analysis

To calculate surface temperature \( T_s \),

\[ P_{loss} = h_{conv}A_s(T_s - T_\infty) + \varepsilon\sigma A_s(T_s^4 - T_{surr}^4) \]

where,

- \( P_{loss} \) - Total Power Loss = 7.1322 W
- \( h_{conv} \) - convection heat transfer co-efficient
- \( A_s \) - Total Surface Area = \((2 \times 35 \times 41 + 2 \times 41 \times 82 + 2 \times 82 \times 25) \times 10^6 = 0.0137 \text{ m}^2\)
- \( T_\infty \) - Temperature of air (sufficiently far away from the surface) = 45°C (assumed)
- \( \varepsilon \) - Surface emissivity for Radiation = 0.6 (assumed)
- \( \sigma \) - Stefan - Boltzmann constant \( (5.67 \times 10^{-8} \text{ Wm}^{-2}\text{K}^{-4}) \)
- \( T_{surr} \) - Surrounding Temperature - 25°C (assumed)

Other than \( h_{conv} \), we have all the other values.

\[ h_{conv} = \frac{Nu \times k}{L_c} \]

where,

- \( Nu \) - Nusselt number
- \( k \) - Thermal conductivity of air = 0.02881 \( \text{ Wm}^{-1}\text{K}^{-1} \)
- \( L_c \) - Characteristic length (Length of vertical surface - Inductor height) = 82mm

To calculate Nusselt Number,

\[ Nu = \left[ 0.825 + \frac{0.387Ra^{1/6}_L}{1 + \left( \frac{0.492}{Pr} \right)^{9/16}} \right]^{8/27} \]

where,
Chapter 3. Hardware Design

RaL - Rayleigh number
Pr - Prandl number = 0.7177

To calculate Rayleigh number,

\[ RaL = \frac{g\beta (T_s' - T_\infty) L^3}{\nu^2} Pr \]

where,

\( \nu \) - kinematic viscosity = 1.995 \times 10^{-5} m^2s^{-1}
\( g \) - Gravitational acceleration = 9.8 ms^{-2}
\( \beta \) - volume expansion coefficient = 1/T_s
\( T_s' \) - Initially assumed surface temperature. (It should match with final solution)

After several iterations, for \( T_s = 88^\circ C \) or 361 K the iteration is converged.

This \( (88^\circ C) \) is the final steady state temperature.

3.2 Switching device selection and Loss calculation

At lower voltage levels, Mosfets having very less conduction losses when compared to IGBTs. So it has been decided to use IRF3710 as switching device. This device is having 23m\( \Omega \) On-state resistance and the 57A of current carrying capability. To reduce the losses much further, 3-devices are paralleled together. Totally each leg has 6-Mosfets so, each inverter contains 18-Mosfets. Loss Calculation below is done for one device.

3.2.1 Conduction Loss

MOSFET Conduction loss: It has been assumed that the current is equally shared by all the three Mosfets,

\[ MOSFET\ Conduction\ Loss = \sum \frac{(I_{pk}\sin\theta)^2 \times 23m\Omega \times d}{f_s/f} \]  

\[ Diode\ Conduction\ Loss = \sum \frac{V_d I_{pk}\sin\theta \times (1 - d)}{f_s/f} \]

summation done between \( \theta = 0^\circ \) to \( 180^\circ \);(for another \( 180^\circ \) bottom switch will be in conduction)

\[ \Delta\theta = \frac{2\pi}{f_s/f} \]
where,
\[ I_{pk} = \frac{50 \times \sqrt{2}}{3} = 23.57 \text{A} \]
\[ d = \frac{m \times \sin(\theta + \phi) + 1}{2} \]
where \( \phi \) - phase difference between current and voltage
\( m \) - modulation index (0.866-maximum)
\( f_s = \) Switching frequency 20kHz; \( f = \) fundamental frequency 50Hz
\( V_d = \) Diode Forward Voltage drop 1.2V

MOSFET loss when \( \phi = 0^0 \) is 2.7713 W & when \( \phi = 90^0 \) loss is 1.5972 W
Diode loss when \( \phi = 0^0 \) is 10.44 W & when \( \phi = 90^0 \) loss is 13.5 W

Maximum Conduction loss of 15.1W occurs when phase difference is at 90°.

### 3.2.2 Switching loss

A small chopper has been built to measure the switching duration of the Mosfet.
\( t_{on} = 100\text{ns} \); \( t_{off} = 500\text{ns} \)

\[ SwitchingLoss = 50 \times \left( \sum \frac{V_{dc} I_{pk} \sin \theta \times (t_{off} + t_{on})}{6} \right) = 1.44W \quad (3.9) \]

summation done between \( \theta = 0^0 \) to 360°;
\[ \Delta \theta = \frac{2\pi}{f_s/f} \]
where,
\[ I_{pk} = \frac{50 \times \sqrt{2}}{3} = 23.57 \text{A} \]
\[ V_{dc} = 48 \text{V} \]

#### 3.2.2.1 Diode Reverse Recovery Loss

Reverse Recovery Charge Stored \( Q_{rr} = 1010nC \) (Worst case datasheet value)
Recovery loss = \( Q_{rr} \times V_{dc} \times f_s = 0.9696W \)

Total Switching loss = Device Switching loss + RR loss = 2.41W
3.2.3 Total Loss

Worst case of total Loss (17.51W) occurs when the current and voltage are at 90°. This is the power loss of a single device. There are totally 18 devices per Inverter. Therefore,

Total Mosfet loss = 18 * 17.51 = 315 W

A Heat sink of $R_{th} = 0.317°C/W$ (without fan) $R_{th} = 0.034°C/W$ (with fan) - has been used. For continuous operation, a fan must be mounted.

3.3 DC bus Capacitor Selection

DC bus ripple current = DC bus RMS current - DC bus Average Current

To calculate both RMS and average currents, we need to know the current profile of the DC bus. i.e., value of the current at all the times.

- As shown in fig.3.4 currents, $I_1, I_2$ and $I_3$ are 120° out of phase.
The conduction device is MOSFET or the BODY DIODE - decided by the CURRENT polarity.

Conducting period is decided by the Switching duty ratio. i.e., by the VOLTAGE modulating wave

When the current is in positive direction, the upper Mosfet conducts in its ON-state.

When the current is in negative direction, the Body Diode conducts in ON-state of Upper device.

For a Sine-Sawtooth modulation, all the upper devices are initially ON and at the End all are in OFF state. From fig.3.4. We sort the current values in ascending order based on the conduction duty ratio.

\[ d_x \leq d_y \leq d_z \]

where, \( d_x, d_y, d_z \) are the duty ratios of three currents in ascending order for each switching cycle.

Now DC bus current

- from 0 to \( d_x \) \( I_{dc} = I_x + I_y + I_z \)
- from \( d_x \) to \( d_y \) \( I_{dc} = I_y + I_z \)
- from \( d_y \) to \( d_z \) \( I_{dc} = I_z \)

after \( d_z \) DC bus current is zero. fig.3.4

Based on the above calculation, we can get the current value and its duration information. From this we can calculate the average and RMS values for various phase angles.

When \( \phi = 0 \) and when the Inductor current is at 50A
\[ I_{ripple} = I_{rms} - I_{dc} = 54.63 - 45.93 = 8.7A \]

When \( \phi = 90 \) and when Inductor current is at 50A
\[ I_{ripple} = I_{rms} - I_{dc} = 24.43 - 0 = 24.3A \]

Where \( \phi \) = phase angle between current and voltage

Therefore, the maximum DC bus current ripple is 24A.

100V, 470\( \mu \)F capacitors with a ripple current capability of 1.065A and with a multiplication factor 1.5(20kHz) has been chosen. Therefore each capacitor can sustain 1.6A ripple
current.
No of capacitors needed = \( \frac{24}{1.6} = 15 \)

Totally 16 parallel connected capacitors are used per inverter.

### 3.3.1 Voltage Ripple

\[
V_{\text{ripple}} = \frac{I_{\text{ripple}}}{16 \times 2\pi f_s C} \tag{3.10}
\]

\[
V_{\text{ripple}} = \frac{24}{16 \times 2\pi \times 200000 \times 470 \times 10^{-6}} = 25.4mV
\]

25.4mV is very less value. So the design is verified.

### 3.4 Sensors Design

#### 3.4.1 Current Sensor

Open loop Hall Effect sensor rated for 200A is used. Since the maximum value of current is 71A, corresponding desired voltage is 5V output from the current sensor. Sensor output is 4V at 200A. So to amplify the voltage signal a non-inverting amplifier is used to get the desired current sensor gain. Fig.3.5

![Current Sensor Diagram](image)
3.4.2 Voltage Sensor

Since the DC bus voltage is only of 48V. It is wiser to use a simple, non-isolated voltage sensor. Initially, the voltage division has been made to bring down the voltage signal within the operating range of op-amp. Then that has been amplified. Fig.3.6

![Figure 3.6: Voltage Sensor](image)

Note: $R_1 \gg R_y$ so that loading effect will not be there. Gain calculation becomes easy.

$$V_{out} = \left( \frac{R_2}{R_1} \right) \ast (V_y - V_x) \quad (3.11)$$

3.5 Modified Delay Circuit

3.5.1 Problem in Existing Protection and Delay Card

As explained in the fig.3.7 Because of the PD card clock, the voltage seen by the inductor is totally different from what we expect. The reason is, on both the sides PWM signals are applied. Generally the case will be one side of the inductor will see a continuous sinusoidal wave (e.g., grid) and only the other side faces the PWM signals.

Here both sides of the inductor faces PWM signals. So Pulse occurring period is very crucial. One possible solution is, increasing the clock frequency. But with existing hardware, the maximum clock signal possible is only 2MHz. But still because of waveform mismatch, lot of noise near the zero crossing and current is not at all a sinusoidal quantity. So closed loop control can not be implemented at all.
Figure 3.7: Existing PD card PWM Signals
3.5.2 Solution

To overcome this problem all the 6-PWM signals are derived from the processor and ANDed with the Enable signal. The Enable signal comes from the Protection and Delay Card. The deadtime has been implemented in software.

Inside the processor, the Event Manager modules contains, the provision to add deadtime. This facility has been utilized. The schematic of additional card used along with the existing Protection and Delay card is shown in fig.3.8.

3.5.2.1 Limitation

Sometimes, the processor may give the output of all PWM signals as ON. This results in dead-short of switching devices. This should be detected and PWM output should be tripped.

![Modified Delay Circuit Diagram](image)

Figure 3.8: Modified Delay Circuit
Chapter 4
Simulation and Digital Implementation

4.1 Simulation Setup

The Schematic of simulation setup is shown in fig.4.1.

Figure 4.1: Simulation setup
• Since the switching frequency is 20kHz. A low pass filter of 2kHz as cut-off frequency has been chosen. \( T_f = \frac{1}{2\pi f} = \frac{1}{2\pi 2000} = 80\mu s \)

• As explained in chapter 2, PI controller time constant \( T_c = \frac{L}{R_a} = \frac{94\mu H}{8m\Omega} = 11.8ms \)

• Since the Triangle maximum is 1V, the Converter gain, \( G = 24 \); and feedback gain \( K_f = 1 \)

• PI controller Gain \( K_c = \frac{R_a T_c}{G T_f} = 0.0492 \)

• Steady state Oscillations are seen in the output. To mitigate that, feed froward filter with cut-off frequency of 20Hz is added in the feed-forward path.

4.2 Digital Implementation

4.2.1 Low Pass Filter Design

Low pass filter in digital domain, \( y[n] = y[n - 1] + k \ast (x[n] - y[n - 1]) \)

where,

\[ \begin{align*}
\text{x[n]} & - \text{Present Input} \\
\text{y[n]} & - \text{Present Output} \\
\text{y[n-1]} & - \text{Past Output} \\
k & - \text{smoothing factor} = \frac{\Delta T}{RC + \Delta T}
\end{align*} \]

Sampling time \( \Delta T = 19.5\mu s \)

4.2.1.1 Feedback Filter

RC time constant = 80\mu s

Therefore Smoothing factor \( k = 0.19677 = 0xC98_{16} \)
4.2.1.2 Feed Forward Filter

RC time constant = 8ms

Therefore Smoothing factor \( k = 2.43 \times 10^{-3} = 0x0028_{H0x3FFF} \)

4.2.2 PI Controller Design

\[ y[n] = y[n-1] + K_c(x[n] - x[n-1]) + K_i \Delta T(x[n]) \]

where, \( K_i = \frac{K_c}{T_c} \)

4.2.2.1 \( K_c \) Calculation

Under Steady State Condition, Th PI controller output is just to overcome the resistance drop in the system.

Inside Processor, Under full load current of \( i_x = 0x3FFF \), The Voltage output from the PI controller is, \( V_{pi} = 106 \times 8m\Omega = 0.848V \)

\( V_d \) or \( V_q \) maximum is = \( 3/2 \times 24 \times 0.866 = 31.2V \)

This maximum is recognised by the processor as 0x3FFF. Therefore, 0.848 V has been recognised as 0x01BD.

As seen by the processor, under steady state condition, for the input of 0x01BD it gets current output of 0x3FFF. This is nothing but the steady state gain ratio of the system,

\[ \frac{i_x}{v_x} = \frac{3FFF_H}{01BD_H} = \frac{GK_f}{R_a} \]

\( \frac{T_c}{T_f} = 20 = 0014_H \)

substitute values from equations 4.1 and 4.2,

\[ K_c = \frac{R_aT_c}{K_fGT_f} = \frac{01BD_H \times 0014_H}{3FFF_H} = \frac{22C4_H}{3FFF_H} \]
4.2. Digital Implementation

4.2.2.2 \(K_i\Delta T\) Calculation

\[
K_i\Delta T = K_c \frac{\Delta T}{T_e} = \frac{22C4\mu F}{3FFF_H} \times \frac{19.5\mu s}{10ms} = \frac{0011_H}{3FFF_H}
\]

4.2.3 Feed forward Gain Calculation

As shown above \(V_d\) or \(V_q\) maximum is 31.2V. As already conveyed, only 10% of voltage drop is allowed across the inductor. If 31.2 is recognised as 3FFF_H then it’s 10% value is 0666_H.

Maximum 10% voltage drop occurs, only when the current at its maximum of 106_A or 3FFF_H. PI controller output at steady state is ideally zero. Therefore, in ideal case (\(R_a = 0\)) feed forward voltage \((\omega L i_q)\) 0666_H only driving the current \(i_q\) to 3FFF_H.

\[
\text{Feed forward Gain} = \omega L = \frac{0666_H}{3FFF_H}
\]

4.2.4 Limiter

As all ready described the \(V_{d\ max}\) is 3.12V. And the \(V_{q\ max}\) should be dynamically calculated. As given by following equation,

\[
V_{q\ max} = \sqrt{31.2^2 - V_{d\ max}^2} \quad (4.4)
\]

\[
V_{q\ max} = \sqrt{3FFF_H^2 - V_{d\ max}^2} \quad (4.5)
\]

4.2.4.1 Sqrt Algorithm

To calculate Square root, the following algorithm has been used. As a initial guess value of 500, it gives correct output in 8 iterations for the range of input (\(a\)) values from 1 to 3FFF_H

\[
x_n = \frac{x_{n-1} + \frac{a}{x_{n-1}}}{2} \quad (4.6)
\]

where,
\(a = \) Number for which sqrt operation to be performed
\(x = \) Sqrt of ‘\(a\)’ after sufficient no of iterations
As explained in the section 3.5.2.1, To protect the devices from accidental dead-short damage. The DC bus voltage is limited to 20V. So all the simulation results and experimental results shown here are for 20V of $V_{dc}$ instead of 48V (designed value).

5.1 Simulation Results

Figure 5.1: Graph1: Modulation Voltage of Inverter leg, Graph2: Current
5.1. Simulation Results

Figure 5.2: Graph1: Modulation Voltage of Inverter leg, Graph2: Current

Figure 5.3: Graph1: Modulation Voltage of Inverter leg, Graph2: Current
Chapter 5. Simulation and Experimental Results

5.2 Experimental Results

Figure 5.4: Graph1: Modulation Voltage of Inverter leg, Graph2: Current

Figure 5.5: Graph1: DC bus Current    Graph2: Inductor Current
5.1. Simulation Results

Figure 5.6: Graph1: Modulation Voltage of Inverter leg, Graph2: Current

Figure 5.7: Graph1: Modulation Voltage of Inverter leg, Graph2: Current
Figure 5.8: Graph1: Modulation Voltage of Inverter leg, Graph2: Current

Figure 5.9: Graph1: Modulation Voltage of Inverter leg, Graph2: Current
5.3 Power Loss

Figure 5.10: Inductor Current vs Power Loss (Experimental)
Chapter 6

Conclusion

The main aim of the project consists of building two High Current Low Voltage Inverters and doing the load test. Both of the aims are fulfilled.

The hardwares built for the project,

- High current Inductors
- Power Circuit Board for placing MOSFET, Capacitor Circuit board for DC bus capacitors
- Non-isolated voltage, Current sensor, New Delay Card

The control is implemented using DSP TMS320F2812 processor.

Future work consists of overcoming the limitation in new Delay Card and Run the inverter at 48V rated condition. The inductance values of inductors are larger than the predicted, so the airgap need to be adjusted. The heat sink is not mounted with a fan. For continuous operation under full rated condition a fan is needed.
References


[9] Data sheets of various chips, devices, capacitors, sensors - Internet