Modulation Strategies for Direct-Link Drive for Open-End Winding AC Machines

Apurva Somani, Ranjan K. Gupta, Krushna K. Mohapatra, Kaushik Basu and Ned Mohan
Department of Electrical and Computer Engineering
University of Minnesota
Minneapolis, MN 55455

Abstract—Switching common-mode voltages generated by conventional pulse-width modulated inverters are known to cause bearing currents in ac machines. These undesirable currents may result in bearing damage. A direct-link drive for open-end winding ac machines has recently been proposed. Some advantages of the drive include: 1) common-mode voltage suppression, 2) no storage elements, and 3) ability to achieve up to 1.5 times the peak input phase voltage across the machine phase windings. In this paper, pulsewidth modulation strategies for the drive are proposed. Two strategies are based on space vector modulation and suppress common-mode voltage at the machine terminals. One carrier-based strategy achieves 1.5 times the peak input phase voltage across the machine phase windings but causes switching common-mode voltage at the machine terminals. Simulation and experimental results are presented to verify the operation of the drive.

I. INTRODUCTION

Pulse-width modulated (PWM) inverters are widely used in variable frequency drives. However, conventional PWM inverters cause switching common-mode voltages at the terminals of ac machines. These switching common-mode voltages are known to cause undesirable bearing currents which may damage the machine bearings [1] [2]. EMI issues also arise due to these common-mode voltages [3]. Methods have been proposed in literature which address this problem. Extra hardware or special modulation strategies are employed to reduce common-mode voltages [4]–[6].

In [7], a direct-link drive for open-end winding ac machines was proposed. The drive has the advantages of:

1) No energy storage components
2) Ability to achieve up to 1.5 times the peak input phase voltage across the machine phase windings
3) Suppression of common-mode voltages at the machine terminals

This topology combined the benefits of the topologies presented in [8] and [9]. In addition to the above advantages, the drive uses 18 unidirectional switches as compared to 36 switches used by the matrix converter based drives in [10] and [11].

Operation of the direct-link drive has been presented in [7]. It is briefly outlined again in Section II. Section III presents three modulation strategies for the direct-link drive. Simulation and experimental results for the drive are presented in Sections IV and V respectively.

II. DIRECT-LINK DRIVE AND ITS OPERATION

The circuit configuration of the direct-link drive is shown in Fig. 1. The front-end rectifier is denoted by ‘RECT’. Its operation is similar to that of a three-phase diode bridge rectifier. Switches (e.g. IGBT’s) with bidirectional current carrying capability are used instead of diodes to allow operation in the generating mode. The top-switch of a phase leg is turned ON when the corresponding phase voltage is maximum. Similarly, the bottom switch is turned ON when the corresponding phase voltage is minimum. The direct-link voltage at the terminals of the ac machine can be limited only certain active vectors of the two inverters, common-mode voltage at the terminal is 120°-conduction waveform with unity displacement power factor. The input power factor of the drive is uncontrollable and the input current has considerable total harmonic distortion (THD ≈ 30%).

The two inverters, shown as ‘INV1’ and ‘INV2’ in Fig. 1, are modulated in synchronism to generate three-phase sinusoidal voltages across the machine phase windings. Due to high switching frequencies of modern drives (5 – 20 kHz), the time-varying nature of the direct-link voltage v_d poses no problem. It has been shown in [7] and [9] that using only certain active vectors of the two inverters, common-mode voltage at the terminals of the ac machine can be limited to a slowly varying waveform. The common-mode voltage is proportional to the direct-link voltage and therefore varies at 360 Hz for a drive with 60 Hz input voltages. This voltage does not have any high frequency components. Thus it is expected that it will not cause any undesirable bearing currents.
III. MODULATION OF DIRECT-LINK DRIVE

The common-mode voltage generated at the terminals of the ac machine can be defined as:

\[
\begin{align*}
v_{CM1} &= \frac{v_{A1N} + v_{B1N} + v_{C1N}}{3} \\
v_{CM2} &= \frac{v_{A2N} + v_{B2N} + v_{C2N}}{3}
\end{align*}
\]  

(1)

It has been shown in [7] and [9] that by using only certain active vectors of the individual inverters, common-mode voltage can be suppressed. In Fig. 3, vectors 1, 3 and 5 have a common-mode voltage of \( v_d/3 \). Vectors 2, 4 and 6 have a common-mode voltage of \( 2v_d/3 \). If only vectors 1, 3, 5 and 1', 3', 5' are used to generate the output voltage, the common-mode voltage at the machine terminals will always be \( v_d/3 \) [9]. The resultant vectors that appear across the machine phase windings are \( OA, OB, \ldots \text{ and } OF \). These are shown in Fig. 3. Using these vectors for output voltage generation does not cause any switching common-mode voltage the machine terminals.

A. Space vector based modulation strategy

The resultant vectors across the open-end windings that do not cause any switching common-mode voltage are shown in Fig. 3. The resultant zero vectors are obtained by applying vectors combinations \( 1 - 1', 3 - 3' \) and \( 5 - 5' \). In sector \( I \), to generate the output voltage vector, vectors \( OA \) and \( OB \) are applied along with the zero vector in a switching time period. To apply the effective vector \( OA \), INV1 should apply vector 1 and INV2 should apply vector 5'. Similarly, to generate vector \( OB \), INV1 should apply vector 3 and INV2 should apply vector 5'. To apply a zero vector, INV1 and INV2 should apply vectors 5 and 5' respectively. Thus it seen that in sector \( I \), INV2 gets clamped to vector 5' and INV1 switches between the vectors 1, 3 and 5 [9].

In this modulation strategy, SVPWM is achieved using \( OA, OB, \ldots \text{ and } OF \) as basic vectors. The switching states are then mapped to the individual inverters INV1 and INV2. The resultant zero vectors are mapped to vectors of the individual vectors depending on the sector information. These mappings are shown in Tables I and II. While implementing space vector modulation on the resultant vectors, the vector lengths are not constant. This is due to the time-varying nature of the direct-link voltage \( v_d \). The direct-link voltage thus needs to be sensed and compensated for. The time-varying voltage does not pose a problem in modulation due to high inverter switching frequencies and fast computational speeds [8].

It should be noted that the resultant vectors are shifted in the counter-clockwise direction with respect to the phase-a axis (Fig. 3). These vectors are rotated by 30°. Thus the reference output voltage vector (\( \vec{v}_{o,ref} \)) also needs to be shifted by 30°. Let the shifted reference voltage vector be denoted by \( \vec{v}'_{o,ref} \). Then,

\[
\vec{v}'_{o,ref} = \vec{v}_{o,ref} e^{j30^\circ}
\]  

(2)

B. Carrier-based modulation

A carrier-based PWM method for the direct-link drive is outlined here. This scheme is easy to implement. It is similar to conventional sine PWM of a three-phase two-level inverter. The control signals of the individual inverters are out of phase by 180°. For a desired effective modulation index of \( m \), the control signals for the two inverters are given by:

\[
\begin{align*}
m_{A1} &= \frac{m}{2} \cos \omega t + \frac{1}{2} \\
m_{B1} &= \frac{m}{2} \cos \left( \omega t - \frac{2\pi}{3} \right) + \frac{1}{2} \\
m_{C1} &= \frac{m}{2} \cos \left( \omega t - \frac{4\pi}{3} \right) + \frac{1}{2} \\
m_{A2} &= -\frac{m}{2} \cos \omega t + \frac{1}{2} \\
m_{B2} &= -\frac{m}{2} \cos \left( \omega t - \frac{2\pi}{3} \right) + \frac{1}{2}
\end{align*}
\]  

(3)

<table>
<thead>
<tr>
<th>Resultant Vector</th>
<th>OA</th>
<th>OB</th>
<th>OC</th>
<th>OD</th>
<th>OE</th>
<th>OF</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV1 Vector</td>
<td>1</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>INV2 Vector</td>
<td>5'</td>
<td>5'</td>
<td>1'</td>
<td>1'</td>
<td>3'</td>
<td>3'</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sector Number</th>
<th>I</th>
<th>II</th>
<th>III</th>
<th>IV</th>
<th>V</th>
<th>VI</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV1 Vector</td>
<td>5</td>
<td>3</td>
<td>1</td>
<td>5</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>INV2 Vector</td>
<td>5'</td>
<td>3'</td>
<td>1'</td>
<td>5'</td>
<td>3'</td>
<td>1'</td>
</tr>
</tbody>
</table>
O as basic vectors are generated within $-\theta$ and $1$, $R - 5 \vec{v} - 120 \text{rms}$ $V R 98 - 5 \cos \left( \theta - \frac{4\pi}{3} \right), \quad (6)$

where $T_s$ is the sampling period, $m_x$ is the modulation index corresponding to $\vec{v}_x$ and $\theta_x$ is the position of $\vec{v}_x$.

IV. SIMULATION RESULTS

The space vector and carrier-based techniques are simulated in Simulink®. The parameters for the simulation are given in Table III. The output voltage command is kept at 1.45 times the input voltage magnitude. For space vector based modulation, vector sets 1, 3 & 5 and 1', 3' & 5' were used for INVI and INV2 respectively.

Fig. 5 shows the output phase voltage and current for space vector PWM based methods. The input phase voltage and current are shown in Fig. 6. The $120^\circ$-conduction nature of the input current is verified. The common-mode voltage at one of the machine terminals $v_{CM1}$ and the common-mode voltage appearing across the machine phase windings are shown in Fig. 7. The common-mode voltage at the terminals is a slowly varying waveform. The frequency of variation is 360 Hz. Since it does not have any high $dv/dt$ components, it is expected that this common-mode voltage will reduce harmful bearing currents as compared to conventional PWM drives. The common-mode voltage across the phase windings is zero.

Simulation results for the carrier-based PWM strategy are presented in Figs. 8-10. It is seen that switching common-mode voltages occur at the machine terminals when using this strategy. Common-mode voltage across the machine phase windings is also not zero. However, the switching cycle average of this voltage is zero and it does not cause any low frequency zero sequence currents.

V. HARDWARE RESULTS

A 5kW prototype has been built and is shown in Fig. 11. Snubber capacitors (total combination of 1.98µF) are used across the direct-link to limit voltage spikes in the direct-link voltage $v_d$. The space vector modulation strategy is implemented on a dSPACE and FPGA-based system. PWM pulses from space vector modulation with the resultant vectors $(OA, OB, \ldots$ and $OF)$ as basic vectors are generated within dSPACE. The mappings shown in Tables I and II are implemented in FPGA. The system parameters of the experimental setup are given in Table IV. The setup is operated at a lower power (about 1kW).

Fig. 12 shows the output phase voltage and current waveforms. The input phase voltage and current are shown in Fig. 13. The input current is $120^\circ$-conduction. The common-mode voltage at one of the terminals is shown in Fig. 14. It is seen

\[
\frac{T_v}{T_s} = \frac{1}{3} - \frac{2}{3} m_x \cos \left( \frac{\theta_x - 2\pi}{3} \right)
\]

\[
\frac{v_{CM1}}{V_{ph}} = \frac{1}{3} - \frac{2}{3} m_x \cos \left( \frac{\theta_x - 4\pi}{3} \right)
\]

Table III

<table>
<thead>
<tr>
<th>System Parameters used for Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input phase voltage, $v_{in}$</strong></td>
</tr>
<tr>
<td><strong>Commanded output phase voltage, $v_{out}$</strong></td>
</tr>
<tr>
<td><strong>Three phase R-L load</strong></td>
</tr>
<tr>
<td><strong>Switching frequency, $f_{sw}$</strong></td>
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</table>
Fig. 5. Output phase voltage ($v_{out}$) and output phase current ($i_{out}$) for space vector-based PWM

Fig. 6. Input phase voltage ($v_{in}$) and input phase current ($i_{in}$) for space vector-based PWM

Fig. 7. Common-mode voltage at machine terminal ($v_{CM1}$) and across phase windings ($v_{CM}$) for space vector-based PWM

Fig. 8. Output phase voltage ($v_{out}$) and output phase current ($i_{out}$) for carrier-based PWM

Fig. 9. Input phase voltage ($v_{in}$) and input phase current ($i_{in}$) for carrier-based PWM

Fig. 10. Common-mode voltage at machine terminal ($v_{CM1}$) and across phase windings ($v_{CM}$) for carrier-based PWM
TABLE IV
SYSTEM PARAMETERS FOR EXPERIMENTAL SETUP

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input phase voltage, $v_{in}$</td>
<td>70 V rms</td>
</tr>
<tr>
<td>Commanded output phase voltage, $v_{out}$</td>
<td>90 V rms</td>
</tr>
<tr>
<td>Three phase R-L load</td>
<td>22.5Ω, 15 mH</td>
</tr>
<tr>
<td>Switching frequency, $f_{sw}$</td>
<td>5 kHz</td>
</tr>
<tr>
<td>Deadtime, $T_d$</td>
<td>5 µs</td>
</tr>
</tbody>
</table>

that the common-mode voltage has switching components. This is due to deadtime used in the inverter legs and is evident in Fig. 15. A deadtime compensation scheme proposed in [13] can be employed to solve this problem.

VI. CONCLUSION

Three modulation strategies for a direct-link drive for open-end winding machines have been presented. Two modulation strategies are space vector modulation based. These strategies do not cause any switching common-mode voltages at the machine terminals. A third carrier-based strategy is outlined which does not address the problem of switching common-mode voltage. All three strategies achieve up to 1.5 times the peak input phase voltage across the phase windings. Simulation and experimental results are presented.

REFERENCES


