A Soft-switched High Frequency link Single-Stage Three-Phase Inverter for Grid Integration of Utility Scale Renewables

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Abstract—A novel single-stage high frequency link three-phase ($3\phi$) inverter along with a modulation strategy is presented in this paper. The topology is targeted for grid integration of utility scale renewable and alternative energy sources such as solar, fuel cell and wind, where the power flow is unidirectional (from DC to AC). The primary side converter has $3\phi$ voltage source inverter (VSI) structure along with an additional half-bridge leg. Sinusoidal pulse width modulation is implemented in the primary side converter. The three legs of the primary side VSI are zero voltage switched (ZVS) for most part of the line cycle. The active switches in secondary side converter are line frequency switched and thus results in negligible switching loss. The converter switching process is described in detail to show the soft-switching of the primary side converter using the device capacitances and leakage inductances of the high frequency transformers. The high frequency transformer galvanic isolation results in high power density. A 4 kW laboratory scale hardware prototype is built and tested with the proposed modulation strategy. The experimental results are presented to verify the converter operation.

Index Terms—Single-stage, high frequency link, DC-AC converter, pulse-width modulation, zero-voltage-switching, line frequency unfolding.

I. INTRODUCTION

WITH the depletion of fossil fuel reserve and the present global warming scenario, power utilities all over the world are focusing on renewable and alternative energy source based power generation. In 2016 globally, total installed renewable power capacity is 921 GW out of which 303 GW is solar capacity and wind power is 487 GW [1]. Commercially available power electronic converters to integrate utility scale (few hundreds of kW to few MW) renewable energy systems to AC transmission grid (Fig. 1a and Fig. 1b) use a three-phase ($3\phi$) voltage source inverter (VSI) in case of PV [2], [3] or back to back connected $3\phi$ VSIs in case of wind [4], [5]. The VSI output is connected to the LVAC (440-480V) grid through line filters and a $3\phi$ line frequency transformer (LFT). Beside the voltage matching the LFT ensures safety by providing galvanic isolation [6], avoiding DC current injection into the grid [7] and also helps to reduce leakage current to conform with the PV system standards such as VDE 0126-1-1 [8]. The LFTs are heavy, bulky and expensive.

High frequency link (HFL) based isolated converter topologies as an alternative solution to LFT based state of the art converters have been studied extensively in recent years. The high frequency transformer (HFT) based solution comes with some attractive features like high power density, small and compact footprint, low system cost. Most popular HFL based solutions are the two-stage HFL DC-AC converter topologies [9]–[13]. In these topologies, an isolated DC-DC stage is connected to a VSI through a DC bus capacitor (Fig. 1c). The intermediate DC bus is voltage stiff. The VSI is high frequency hard-switched and the DC electrolytic capacitor has long term reliability issue [14]. The VSI can be soft-switched by employing additional switches and resonating inductors and capacitors in the DC link. The resonant DC link concept is first introduced in [15] where a LC network is used to produce oscillatory DC link voltage and the inverter is switched when the DC link voltage becomes zero. The inverter switches suffer from high voltage stress (2-3 times input DC voltage) and discrete pulse modulation (sigma-delta) strategy produces significant undesirable sub-harmonics at the output, [15], [16]. In quasi-resonant DC link inverter (QRDCLI), the resonating circuit comes in operation only during the switching transitions of the inverter to make the link voltage zero. The first QRDCLI topology was proposed in [17], where the resonating circuit has four active switches. Subsequent works [18]–[22], tried to address the problem of high voltage and current stress experienced by the additional switches in the resonant cell and to reduce the number of the active devices. [19], [20], [23] reduced the frequency of the operations of the resonant cell, by reducing the number of switching transitions through modification of the PWM strategies of the inverter. This approach usually results in low quality output voltage waveform when compared with standard conventional space vector PWM. In general, the QRDCLI uses at least one active switch in series with the DC voltage source to disconnect the supply during resonant operation. The RMS and peak current rating of this switch is significantly high compared to the inverter switches. Though soft-switched, this switch contributes significantly to the conduction loss. This restricts the use of QRDCLI in high power application. Additionally, control complexity and high current stress of resonant circuit...
are two major limitations of QRDCLI.

In literature single-stage rectifier type HFL DC-AC converters (RHFL) are widely discussed where inter-stage DC capacitor is removed (Fig. 1d) and the DC bus is pulsating [24]–[27].

The DSC leg ($S_{ij}$) is zero voltage switched (ZVS) over a complete line cycle where as other three legs are zero voltage (ZVS) switched for most part of a line cycle.

The high frequency galvanic isolation provides a compact high power density converter solution.

A part of this work was presented in [33].

The paper is organised as follows. Section II describes the modulation strategy of the converter. In section III, the converter switching process is described in detail. Experimental results are presented in section IV to validate the theoretical analysis. The converter power loss and efficiency are presented in section V.

II. CIRCUIT CONFIGURATION AND MODULATION TECHNIQUE

The proposed topology is shown in Fig. 2a. The primary side of the converter has a two level three-phase ($3\phi$) voltage source inverter (VSI) structure connected to the DC source $V_{dc}$ along with one additional half-bridge leg ($S_1-S_2$). For each phase, a three winding high frequency transformer (HFT) with turns ratio ($n:1:1$) is employed. The primary windings of the $3\phi$ HFTs are star connected and the neutral point ($N$) is connected to the pole of leg $S_1-S_2$. In each phase, the starting end of one secondary winding is connected to the finishing end of the other identical secondary winding. All these points are connected to form a common point ($n_1$). In the secondary side, each phase of the converter has a diode bridge along with a half-bridge leg. The converter is connected to a balanced $3\phi$ voltage source ($v_u,v_v,v_w$) with angular frequency $\omega_o = \frac{2\pi}{T_o}$ and peak $V_{gpk}$ through filter inductors ($L_f$). All the active switches can be realized with IGBT or MOSFET with a body diode. In the following discussion, IGBTs are considered for implementation. The directions of the currents shown in Fig. 2a are considered to be positive in rest of the paper.

To generate balanced adjustable magnitude $3\phi$ AC from the input DC, the modulation signals ($m_{ij}^*$) are given in (1).

$$m_{ij}^* = m \left| \sin \left( \omega_o t + M_j \frac{2\pi}{3} \right) \right|$$

Due to presence of diode bridge, the instantaneous power flow is unidirectional (from DC to AC). The carrier frequency average of the synthesized pole voltages ($\overline{v_{pn}}$) should be in phase with the fundamental component of line currents ($i_{a,b,c}$) (Fig. 2a). So, the reference signals ($m_{ij}^*$) are in phase with fundamental component of the line currents, $i_j$. The modulation is implemented in the primary-side converter. The eight switches in the DC side converter are modulated following the principle of phase-shifted full-bridge (PSFB) DC-DC converter. A high frequency square wave signal $f$ with time period $T_s$ and duty ratio 0.5 is considered, Fig. 2b. $T_s$ is also the period of the HFT flux balance cycle. A unipolar saw-tooth carrier with unity peak and period of $\frac{T_s}{2}$ is considered and is aligned with $F$. Each half-bridge leg in the primary is complementary switched with 50% duty ratio. $F$ is used as the gating pulse ($G_{S_{ij}}$) of $S_1$. The gating pulses ($G_{S_{ij}}$) of the top switches of each VSI leg, $S_{X1}$ ($X \in \{A,B,C\}$) are time shifted with respect to $S_1$. For example, $G_{S_{A1}}$ is time delayed by $m_{ca}^* \frac{T_s}{2}$ with respect to $G_{S_1}$ or $F$, Fig. 2b.

So, a sine pulse width modulated (PWM) quasi square wave with levels $\pm V_{dc}$ and zero and period $T_s$ is applied across the transformer primary ($v_{an}$ in Fig. 2b). The high frequency quasi-square wave is rectified by the secondary diode bridges $D_{j1-4}$. When $i_j > 0$, $Q_{j3}$ is turned ON and the high frequency rectification happens with the top diodes $D_{j1}, D_{j3}, Q_{j2}, D_{j2,4}$.
considered as constant current sources with magnitude $I$ for ease of analysis, slowly varying line currents switch at line frequency incurred negligible switching loss. This results in generation of unipolar sine PWM pole voltages $v_{jn}$, with voltage levels 0 and $\pm \left( \frac{V_{dc}}{n} \right)$ with respect to $n_t$ (see $v_{an}$ in Fig. 2c). The average 3φ pole voltages with respect to HFT secondary neutral $n_t$ are given in (2).

$$\overline{v}_{jn} = \frac{mV_{dc}}{n} \sin \left( \omega_c t + M_j \frac{2\pi}{3} \right) \quad (2)$$

For a desired average pole voltage peak, $V_{pk}$, the modulation index $m = \left( \frac{nV_{pk}}{V_{dc}} \right)$. As the AC ports are connected to a balanced 3φ system with floating neutral ($n_y$), the average pole voltages $\overline{v}_{jn}$ are equal to output voltages $\overline{v}_{jn}$.

III. CONVERTER SWITCHING PROCESS

In this section, the circuit operation of the converter is discussed in detail over one switching cycle ($T_s$). The presented analysis shows that the half-bridge leg $S_1 - S_2$ is completely soft-switched and each of the legs of the VSI, $S_{X1} - S_{X2}$ ($X \in \{A, B, C\}$), are soft-switched for most part of the line cycle with the help of device parasitic capacitances ($C_s$) and transformer leakage and additional series inductance ($L_{lk}$). The secondary side active switch pairs $Q_{j1} - Q_{j2}$ are line frequency switched incurring negligible switching loss. For ease of analysis, slowly varying line currents $i_{a,b,c}$ are considered as constant current sources with magnitude $I_{a,b,c}$ over a switching cycle $T_s$. The switching process of the converter is described when $i_a = I_a$ and $i_b = I_b$ but $i_c = -I_c$ and $I_a > I_b > I_c$. In other regions similar switching process will be followed. Switching waveforms over $T_s$ are shown in Fig. 3. The circuit dynamics in one half of the switching cycle ($T_s$) is divided into ten modes (1-10), other half evolves in an identical fashion.

A. Mode 1 ($t_0 < t < t_1$)

In this mode in the primary side converter, $S_1$ and $S_{X2}$ ($X \in \{A, B, C\}$) are conducting (Fig. 4). The equivalent circuit is shown in Fig. 5a. Negative voltage $-V_{dc}$ is applied across HFT primary terminals $AN$, $BN$ and $CN$. The HFT primary currents, $i_{pj} = -\frac{I_j}{p}$ where ($j \in \{a, b, c\}$) as shown in Fig. 3. The voltage polarity and direction of currents indicate active power flow from DC to AC side in all three phases (all three phases are in active state). In secondary $D_{a3}, Q_{a1}; D_{b3}, Q_{b1}$ and $D_{c2}, Q_{c2}$ are conducting.

B. Mode 2 ($t_1 < t < t_2$)

At $t_1$, $S_{B2}$ is turned OFF (Fig. 6). Active to zero state transition of phase $b$ starts at $t_1$. Due to device capacitance ($C_s$), the voltage across $S_{B2}$ can not rise immediately. Voltage starts rising after channel current falls below zero reaching zero voltage turn OFF (ZVS) of $S_{B2}$, phase primary current $-\frac{I_b}{n}$ starts charging the capacitance across $S_{B2}$ and discharging the capacitance across $S_{B1}$. Equivalent circuit in this mode...
Fig. 3. Switching waveforms over $T_s$

Fig. 4. Simplified circuit diagram in Mode 1 ($t_0 < t < t_1$ in Fig. 3)

is shown in Fig. 5b. From the equivalent circuit it can be shown that the voltages across $S_{B1}$, $v_{S_{B1}}$ falls as per (3).

$$v_{S_{B1}}(t) = V_{dc} - \frac{I_b}{2nC_s}(t - t_1)$$

(3)

Phase $a$ and $c$ remain in active state during this duration.

C. Mode 3 ($t_2 < t < t_3$)

At $t_2$, the capacitor across $S_{B1}$ is completely discharged. The anti-parallel diode of $S_{B1}$ starts conducting (Fig. 7). After $t_2$, $S_{B2}$ blocks $V_{dc}$. The duration $t_{azb} = (t_2 - t_1)$ is given in (4).

$$t_{azb} = \frac{2nC_sV_{dc}}{I_b}$$

(4)

The primary of $b$ phase HFT is shorted through $S_1$ and anti-parallel diode of $S_{B1}$. To achieve ZVS transition, $S_{B1}$ is turned ON in this mode (dead time between $S_{B2}$ and $S_{B1}$ must be greater than $t_{azb}$). Equivalent circuit in this mode is shown in Fig. 8a. Phase $b$ is in zero state i.e no active power is transferred from DC to AC side in phase $b$.

D. Mode 4-6

Similar active to zero state transitions occur in phase $a$ in Mode 4 ($t_3 < t < t_4$) with ZVS turn OFF of $S_{A2}$ and in phase $c$ in Mode 6 ($t_5 < t < t_6$) with ZVS turn OFF of $S_{C2}$. In Mode 5 ($t_4 < t < t_5$), phase $a$, $b$ are in zero states and phase $c$ is in active state. $S_{A1}$ is turned ON to ensure ZVS when its anti-parallel diode is conducting.
Fig. 8. (a) Equivalent circuit diagram in Mode 3, (b) Equivalent circuit diagram in Mode 7.

Fig. 9. Simplified circuit diagram in Mode 7 ($t_6 < t < t_7$ in Fig. 3)

**E. Mode 7 ($t_6 < t < t_7$)**

In this mode, all three phases are in zero state. HFT primary terminals $AN, BN$ and $CN$ are shorted through $S_1$ and the anti-parallel diodes of $S_{X1}$ (Fig. 9). ZVS turn ON of $S_{C1}$ is achieved in this interval. No active power is transferred from DC to AC side. Equivalent circuit is shown in Fig. 8b.

**F. Mode 8 ($t_7 < t < t_8$)**

Fig. 10. Simplified circuit diagram in Mode 8 ($t_7 < t < t_8$ in Fig. 3)

**G. Mode 9 ($t_8 < t < t_9$)**

From (6), $|i_{pj}(t_7)| - |i_{pj}(t_8)|$ have same values for $j = a, b, c$. So, $|i_{pc}(t_8)| > |i_{pa}(t_8)| > |i_{pb}(t_8)|$ as $I_a > I_b > I_c$. In this mode, the primary currents $i_{pj}$ change the direction linearly and whenever $i_{pj}$ reach $I_j$ the circuit dynamics of the corresponding phase is complete. Based on the magnitude at $t_8$, first $b$ phase primary current reaches $I_b$ and then $a$ and then $c$ phase primary currents reach $I_a$ and $I_c$ respectively (see Fig. 12). Mode 9 is divided into three sub-modes. As the primary side 3/6 VSI switches $S_{A1,B1,C1}$ are already ON (ZVS) before entering into this mode, in the sub-modes initially the anti-parallel diodes and then active switches ($S_{A1,B1,C1}$) take part in conduction based on the direction of $i_{pj}$.

At $t_7$, $S_1$ is turned OFF. Due to device capacitance $C_s$, voltage across $S_1$, $v_{S1}$ can not rise immediately, resulting in ZVS turn OFF of $S_1$. The neutral current $i_N$ starts charging the capacitor ($C_s$) across $S_1$ and discharging the capacitor across $S_2$ (Fig. 10). Equivalent circuit in this mode is shown in Fig. 11a. A positive voltage appears across the HFT primaries ($AN, BN$ and $CN$). Secondary diodes $D_{a1}, D_{b1}$ and $D_{c4}$ are forward biased and start conducting. This results in shorting of HFT secondary windings (Fig. 11a) and the primary circuit dynamics become independent of secondary line currents. In primary, the voltage polarity is against the direction of currents through $L_{ik}$ resulting in reduction of magnitudes of primary currents ($i_{pa}, i_{pb}$ and $i_{pc}$). Circuit equations are given in (5).

$$i_N = i_{pa} + i_{pb} + i_{pc}$$

$$V_{dc} = v_{S1} + v_{S2}$$

$$i_N(t) = C_S \left( \frac{dv_{S1}}{dt} - \frac{dv_{S2}}{dt} \right)$$

(5)

$$\frac{dv_{S1}}{dt} = \frac{d}{dt} \left( i_{pa} + i_{pb} + i_{pc} \right)$$

$$\frac{dv_{S2}}{dt} = \frac{d}{dt} \left( i_{pa} + i_{pb} + i_{pc} \right)$$

Where $v_{S1}$ and $v_{S2}$ are the voltages across $S_1$ and $S_2$. Solving (5) following expressions of voltage and currents are obtained.

$$i_N(t) = i_N(t_7) \cos \omega_r(t - t_7)$$

$$i_{pj}(t) = i_{pj}(t_7) - \frac{i_N(t_7)}{3} (1 - \cos \omega_r(t - t_7))$$

(6)

$$v_{S1}(t) = \frac{\omega_r L_{ik} i_N(t_7)}{3} \sin \omega_r(t - t_7)$$

Where $j \in \{a, b, c\}$ and $\omega_r = \sqrt{\frac{3}{2 L_{ik} C_s}}$. At $t_8$, $v_{S1}$ reaches $V_{dc}$ and $v_{S2} = 0$. The anti-parallel diode of $S_2$ is forward biased and starts conducting. The duration of Mode 8, $t_{za1} = (t_8 - t_7)$ is expressed as

$$t_{za1} = \frac{1}{\omega_r} \sin^{-1} \left( \frac{3V_{dc}}{\omega_r L_{ik} i_N(t_7)} \right)$$

(7)

For the capacitor across $S_2$ to be completely discharged following condition must be satisfied

$$\omega_r L_{ik} i_N(t_7) \geq 3V_{dc}$$

(8)

Else the circuit will enter into resonant oscillation mode with angular frequency $\omega_r$ and will remain in this mode till the gating pulse of $S_2$ is being applied.
In secondary, line currents are transferred linearly from \( D_{a3} \), \( D_{b3} \) and \( D_{c2} \) to \( D_{a1} \), \( D_{b1} \) and \( D_{c4} \) respectively. In Fig. 12, currents through \( D_{a1} \) and \( D_{a3} \) are shown. In this interval \( i_{pb} \) changes its direction.

2) **Sub-mode 2** \((t_{s1} < t < t_{s2})\): At \( t_{s1} \), \( i_{pb} \) reaches the active state value \( \frac{I_b}{n} \). In secondary, \( I_b \) is completely transferred from \( D_{b3} \) to \( D_{b1} \) and \( D_{b3} \) is reverse biased (Fig. 15).

In secondary, \( i_N(t) \) changes from \( \frac{3V_{dc}}{L_{lk}} \) to \( \frac{2V_{dc}}{L_{lk}} \) in this interval. Phase \( b \) has completed its zero to active state transition. Other two primary phase currents changes with same slope as in **Sub-mode 1**.

3) **Sub-mode 3** \((t_{s2} < t < t_9)\): At \( t_{s2} \), \( i_{pa} \) reaches the active state value \( \frac{I_a}{n} \). In secondary, \( I_a \) is transferred completely from \( D_{a3} \) to \( D_{a1} \) and \( D_{a3} \) is reverse biased (Fig. 16). Equivalent circuit is shown in Fig. 14a. As \( i_{pb} \) is clamped to \( \frac{I_b}{n} \), the slope of \( i_N \) changes from \( \frac{3V_{dc}}{L_{lk}} \) to \( \frac{2V_{dc}}{L_{lk}} \) in this interval. Phase \( b \) has completed its zero to active state transition. Other two primary phase currents changes with same slope as in **Sub-mode 1**.
mode 8-9, $i_N$ is changed from $- \frac{I_a + I_b + I_c}{n}$ to $\frac{I_a + I_b + I_c}{n}$. $i_N$ reaches zero at $t_N$ (see Fig. 12). To achieve ZVS turn ON of $S_2$, it must be turned ON in some time between $t_8$ and $t_N$ when the anti-parallel diode of $S_2$ is in conduction. So, it is important to find minimum of $(t_N - t_7) = (t_N - t_8) + (t_8 - t_7)$. $(t_8 - t_7)$ is given in (7). $\Delta t_N$ is defined as $\Delta t_N = (t_N - t_8)$. The objective of the following analysis is to find $\Delta t_{N, \text{min}}$. In this analysis, $(t_8 - t_7)$ and the change in current magnitude, $|i_p(t_7) - i_p(t_8)|$ are considered to be negligible. So, $\Delta t_N$ depends on $m_s$, $I_a$, $I_b$ and $I_c$. Assuming negligible current ripple, the line currents are given as $i_j = I_{pk} \sin \left( \omega_s t + M_j \frac{2\pi}{3} \right)$ (from (1)). So, $\Delta t_N$ depends on $I_{pk}$ and $\alpha$ where $\alpha = (\omega_s t - 90^\circ)$. Let, $i_{\text{max}}$ is maximum of $I_a$, $I_b$ and $I_c$. Similarly, $i_{\text{mid}}$ and $i_{\text{min}}$ can be defined. As $i_a + i_b + i_c = 0$, $i_{\text{max}} = i_{\text{min}} + i_{\text{mid}}$. The waveforms of $i_{\text{pa}}$ and $i_N$ are square waves at switching frequency $T_s$ and have envelopes as $i_{\text{pa}}$ and $i_N$, respectively over a line cycle ($\theta = \omega_s t$) as shown in Fig. 17. $i_{\text{max}}$ has similar envelope as the positive half of $i_N$. Due to symmetry, the analysis of $\Delta t_{N, \text{min}}$ is carried out for $0^\circ < \alpha < 30^\circ$. From above assumption, $i_N(t_8) = - \frac{2i_{\text{max}}}{n}$. The time interval of $\text{Sub-mode \ 1}$ can be expressed as $t_8 - t_8 = \frac{2i_{\text{min}}}{nm_s}$. At $t_8$, $i_N(t)$ can be expressed as in (10).

\[
i_N(t_8) = -\frac{2(i_{\text{max}})}{n} + 3m_s \left( \frac{2i_{\text{min}}}{nm_s} \right)
\]

\[
= \frac{I_{pk}}{n} \left( 3\sqrt{3} \sin \alpha - \cos \alpha \right)
\]

$i_N(t_8)$ is monotonic in $\alpha$ and reaches zero at $\alpha^* = 10.89^\circ$. So, for $\alpha < \alpha^*$, $\Delta t_N$ is given in (11).

\[
\Delta t_N = \frac{2i_{\text{max}}}{n} \left( \frac{1}{3m_s} \right)
\]

\[
= \frac{2I_{pk}}{3nm_s} \cos \alpha \quad 0^\circ < \alpha < \alpha^*
\]

For $\alpha > \alpha^*$, it is possible to show $i_N$ will reach zero in $\text{Sub-mode \ 2}$. $i_N$ will take $\frac{i_N(t_8)}{2m_s}$ amount of time to become zero in $\text{Sub-mode \ 2}$. $\Delta t_N$ is given in (12).

\[
\Delta t_N = \left( \frac{2i_{\text{min}}}{nm_s} \right) + \left( \frac{i_N(t_8)}{2m_s} \right)
\]

\[
= \frac{I_{pk}}{nm_s} \sin(\alpha + 30^\circ) \quad \alpha^* < \alpha < 30^\circ
\]

From (11) and (12), $\Delta t_{N, \text{min}}$ occurs at $\alpha = \alpha^*$ and $\Delta t_N = 0.655 \frac{I_{pk}}{nV_{dc}}$. To achieve ZVS turn ON of the primary half-bridge leg $S_1 - S_2$ over the complete line cycle, the dead-time, $DT$ should be less than $\Delta t_{N, \text{min}}$. Using (7), complete soft-switching condition of $S_1 - S_2$ is given in (13).

\[
\frac{1}{\omega_r} \sin^{-1} \left( \frac{\sqrt{3}nV_{dc}}{\omega_r L_{tk}I_{pk}} \right) \leq DT \leq 0.655 \frac{I_{pk}L_{tk}}{nV_{dc}}
\]

H. Mode 10 ($t_9 < t < t_{10}$)

At $t_9$, $i_{pc}$ reaches the active state value $I_c$. In secondary, $I_c$ is transferred completely from $D_{c2}$ to $D_{c3}$ and $D_{c2}$ is reverse biased (Fig. 18). Equivalent circuit is shown in Fig. 19. All the phases are in active state and transferring power. The circuit configuration is similar as in Mode 1.

In above discussion, polarity reversal of HFT primary voltages and currents are shown in one half of the switching cycle. Similar switching sequence will be followed in rest half of the switching cycle with other symmetrical switches. It is seen that during active to zero state transitions $3\phi$ VSI legs are switched. And the half-bridge leg $(S_1 - S_2)$ is switched during zero to active state transition. The above discussion shows, all switches in the $3\phi$ VSI are zero voltage switched (ZVS) for most part of the line cycle whereas the ZVS of the half-bridge leg $(S_1 - S_2)$ can be ensured over complete line cycle.

IV. EXPERIMENTAL VALIDATION

A. Setup and operating condition

The modulation strategy and switching process of the proposed topology (Fig. 2a) are experimentally verified in a laboratory scale hardware prototype (Fig. 20). Four primary HF legs and three secondary line frequency switched legs are implemented using 1200 V, 75 A SEMIKRON IGBT modules SKM75GB123D. 1200 V, 75 A IXYS fast recovery diode modules MEE 75-12 DA are used to implement secondary.
diode bridges. The IGBT modules are driven with optically isolated gate driver IC, ACPL 339J with driving voltage level ±15 V. The primary modules are switched at 20 kHz whereas the secondary modules are switched at 50 Hz. A 600 ns dead time (DT) is provided between the gating pulses of the top and the bottom IGBTs of an IGBT module. EPCOS ferrite E cores (E 80/38/20) are used for three winding HFTs. The turns ratio is selected as 51:34:34. The leakage inductance of HFTs are in the range of 6-8 μH. A series inductance of 48 H is connected in the range of 6-8 μH.

TABLE I
OPERATING CONDITION OF THE 3φ TOPOLOGY

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Power, P</td>
<td>4 kW</td>
</tr>
<tr>
<td>DC input, Vdc</td>
<td>350 V</td>
</tr>
<tr>
<td>output voltage peak , Vgpk</td>
<td>200 V</td>
</tr>
<tr>
<td>Output frequency, fo</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Switching frequency, f_s</td>
<td>20 kHz</td>
</tr>
</tbody>
</table>

The voltage at point a', b', c' are sensed and modulation index (m) and the phase angle (ϕ) are adjusted for a given power flow (P) to synthesized converter output voltage \( V_{gpk} \). For the operating condition given in Table I, modulation index and phase angle are calculated as \( ϕ = 3^\circ \), \( m = 0.86 \). So, power factor \( \cos ϕ = 0.998 \approx 1 \).

Solving (14),

\[
V_{pk} = \left( \frac{V_{gpk}^2}{2} + \sqrt{\frac{V_{gpk}^4}{4} - \left(\frac{X_P}{1.5}\right)^2} \right)^{1/2}
\]

\[
ϕ = \sin^{-1} \left( \frac{2πfL_fI_{pk}}{V_{gpk}} \right)
\]

The voltage at point a', b', c' are sensed and modulation index (m) and the phase angle (ϕ) are adjusted for a given power flow (P) to synthesized converter output voltage \( V_{gpk} \). For the operating condition given in Table I, modulation index and phase angle are calculated as \( ϕ = 3^\circ \), \( m = 0.86 \). So, power factor \( \cos ϕ = 0.998 \approx 1 \).

B. Verification of modulation strategy

The output of the converter is connected to a balanced 3φ voltage source \( (V_{a'n}, V_{b'n}, \text{ and } V_{c'n}) \) with phase peak \( V_{gpk} \) 200 V and frequency 50 Hz. The converter is modulated to generate balanced 3φ average output voltages \( \bar{V}_{an}, \bar{V}_{bn}, \text{ and } \bar{V}_{cn} \) at 50 Hz following the strategy described in section II so that it supplies active power of 4 kW at unity power factor. \( V_{an} \) leads \( V_{a'n} \). As the impedance of \( L_f = 2.5mH \) at 50 Hz is relatively small, \( \bar{V}_{an} \) approximately follows \( V_{a'n} \).

In Fig. 22a, the pulse width modulated HF AC across HFT primary of phase a (\( v_{AN} \)) is shown. \( v_{AN} \) has voltage levels of
$\pm 350$ V and zero. The unipolar PWM pole voltage ($v_{an_i}$) with respect to HFT secondary neutral $n_t$ is also shown in CH2. $v_{an_i}$ has voltage levels of $\pm 233$ V and zero. The experimental waveforms of $v_{AN}$ and $v_{an_i}$ have matched with the analytical waveforms shown in Fig. 2c. The pole voltage ($v_{an_q}$) with respect to load neutral $n_t$ is presented in CH3. Due to presence of HF common mode voltage, the waveforms of $v_{an_i}$ and $v_{an_q}$ are different though they have same average component. The load voltage waveform ($v_{an_q}$) after line filter $L_f$ is shown in CH4. As in table I, $v_{an_q}$ has a peak value ($V_{gpk}$) of 200 V.

Fig. 22b shows load voltage of phase $a$, $v_{an_q}$ and balanced $3\phi$ line currents $i_{a,b,c}$ over two line cycles. $v_{an_q}$ is almost in phase with $i_a$ and the line currents contain very low high frequency ripple due to filtering action of $L_f$. The line currents have an estimated peak of $I_{pk} = \frac{1.5V_{gpk} \cos \phi}{P}$ = 13.33 A. Experimentally measured peak is 13.4 A. These set of results confirm the three phase operation of the proposed converter.

Line frequency switching of secondary switches are shown in Fig. 23a. The gate emitter voltage of $Q_{a1}$ ($v_{GE,Q_{a1}}$) is high (+15 V) when the line current $i_a > 0$. This experimental result validates line frequency switching described in the modulation strategy and shown in Fig. 2c. Fig. 23a also presents the primary current corresponding to phase $a$ ($i_{pa}$) and the HFT neutral current $i_N$ over a line cycle. The waveform of $i_{pa}$ is high frequency square wave with magnitude sinusoidally varying over line cycle. The envelope of $i_{pa}$ has a peak of $i_{pa,pk} = \frac{I_{pk}}{n} = 8.9$ A. Unlike $i_{pa}$, the envelope of $i_N$ never becomes zero. The envelope of $i_N$ has a periodicity of $\frac{T_0}{6}$ with peak value $i_{N,pk} = 2i_{pa,pk} = 17.8$ A and minimum value $\frac{\sqrt{3}i_{N,pk}}{2} = 15.4$ A. Such envelope of $i_N$ helps to achieve complete soft-switching of leg $S_1-S_2$ over a line cycle.

Fig. 23b presents HFT primary voltage ($v_{AN}$) and current ($i_{pa}$) waveforms over two switching cycle ($2T_s$). HFT primary current polarity changes when applied voltage changes from zero to $\pm V_d$ (zero to active state) as discussed in section III and shown in Fig. 3. Fig. 23b confirms that HFT flux balance is achieved in one switching cycle.

Fig. 24a shows $3\phi$ primary voltages ($v_{A,B,C−N}$) of HFTs along with neutral current $i_N$ over two switching cycles. The experimental waveforms are matched with the analytical waveforms shown in Fig. 3. From the figure, the zero to active state transition occurs simultaneously in all the three phases and during this time $i_N$ also changes its direction. The leg $S_1−S_2$ are switched at this instant. Active to zero transitions are not synchronised.

### C. Verification of converter switching process

The switching strategy of phase legs $S_{A1−A2}$, $S_{B1−B2}$ and $S_{C1−C2}$ are similar. Hence phase $A$ leg $S_{A1−A2}$ are considered for discussion. In a high frequency switching cycle ($T_s$), $S_{A1−A2}$ are switched twice during active to zero state transitions of phase $A$. During one transition $S_{A2}$ is turned ON and $S_{A1}$ is turned OFF and in the next transition $S_{A2}$ is turned OFF and $S_{A1}$ is ON. The switching process in both the transitions are same. Similarly, in a switching cycle ($T_s$) there

---

*Fig. 23. (a) Line frequency switching of secondary switch- [CH1] $v_{GE,Q_{a1}}$ (25V/div.), [CH2] $i_a$ (35A/div.), [CH3] $i_{pa}$ (35A/div.), [CH4] $i_\phi$ (35A/div.). Time scale 2ms/div. (b) HFT primary voltage and current- [CH1] $v_{AN}$ (250V/div.), [CH2] $i_{pa}$ (10A/div.). Time scale 10\mu s/div.*

*Fig. 24. (a) HFTs input voltages and neutral current- [CH1] $v_{AN}$ (500V/div.), [CH2] $v_{BN}$ (500V/div.), [CH3] $v_{CN}$ (500V/div.), [CH4] $i_N$ (20A/div.). Time scale 10\mu s/div. (b) Converter primary currents- [CH1] $i_{pa}$ (5A/div.), [CH2] $i_{pb}$ (5A/div.), [CH3] $i_{pc}$ (5A/div.), [CH4] $i_N$ (5A/div.). Time scale 1\mu s/div.*
are two zero to active state transition during which leg $S_1 - S_2$ are switched. And here also, the switching process wise both the transition of $S_1 - S_2$ is similar. So, it is sufficient to check any one transition in legs $S_{A1} - S_{A2}$ and $S_1 - S_2$ to verify the soft-switching process.

Fig. 25. Switching transition waveforms of leg $S_1 - S_2$ (a) turn ON of $S_1$, (b) turn OFF of $S_2$. Switching transition waveforms of leg $S_{A1} - S_{A2}$ (c) turn ON of $S_{A1}$, (d) turn OFF of $S_{A2}$

In Fig. 25a shows the turn ON transition of $S_1$. It is seen
from the figure that the collector emitter voltage $v_{CE,S_1}$ first falls to zero and the pole current $i_N$ is negative which indicates the anti parallel diode of $S_1$ is in conduction. Before the direction of $i_N$ is changed, the gate-emitter voltage $v_{GE,S_1}$ is applied to achieve zero-voltage turn ON of $S_1$. Fig. 25b shows the turn OFF transition of $S_2$. It is seen that the voltage across $S_2$, $v_{CE,S_2}$ starts rising some time after the removal of the gating pulse, $v_{GE,S_2}$ (when $v_{GE,S_2}$ is approximately zero or is negative). The $v_{GE,S_2}$ represents the channel current of $S_2$. Below threshold voltage the channel current is zero. Due to presence of capacitance across $S_2$ the channel current falls first and then the voltage across $S_2$ starts rising which results in zero voltage turn OFF of $S_2$. These results show the ZVS operation of $S_1 - S_2$.

Fig. 25c shows the turn ON transition of $S_{A1}$. From the figure it is seen that the gating pulse $v_{GE,S_{A1}}$ is applied after the collector emitter voltage $v_{CE,S_{A1}}$ becomes zero. As the pole current ($i_{pa}$) direction does not change during the transition, the anti-parallel diode of $S_{A1}$ is in conduction. So the turn ON of $S_{A1}$ is a zero voltage transition. In Fig. 25d the turn OFF transition of $S_{A2}$ is shown. The collector emitter voltage ($v_{CE,S_{A2}}$) starts rising some time after the gating pulse $v_{GE,S_{A2}}$ is removed and when $v_{GE,S_{A2}}$ is approximately zero or negative. This indicates the channel current through $S_{A2}$ is zero when $v_{CE,S_{A2}}$ starts rising, results in zero voltage turn OFF transition. The delay in rise of $v_{CE,S_{A2}}$ is caused by the capacitance presents across $S_{A2}$. These results show the ZVS operation of $S_{A1} - S_{A2}$.

The $S_{A1} - S_{A2}$ are hard switched in the shaded zone shown in Fig. 17. Fig. 26 presents the hard turn ON of $S_{A1}$. The magnitude of $i_{pa}$ is very low. After the gating pulse of $S_{A2}$, $v_{GE,S_{A2}}$ is removed, the voltage across $S_{A1}$, $v_{CE,S_{A1}}$ starts falling linearly. A sharp fall in $v_{CE,S_{A1}}$ is observed when the $S_{A1}$ is turned ON before the device capacitance $C_s$ is completely discharged. This results in hard turn ON of $S_{A1}$.

V. CONVERTER POWER LOSS AND EFFICIENCY

In this section, power loss of different stages of the converter is estimated and also obtained experimentally for a variation of load power in the range of 1kW-4kW.
A. Analytical loss estimation of the converter

The conduction loss in switch pair $S_1 - S_2$ is given as-

$$P_{C_{S_1}} = P_{C_{S_2}} = \frac{3 V_{CE,S_1,2} I_{pk}}{n \pi} + 1.827 \frac{R_{CE,S_1,2} I_{pk}^2}{n^2}$$

(16)

Where $V_{CE,S_1,2}$ and $R_{CE,S_1,2}$ are constant voltage drop (1.4V) and on state resistance (22mΩ) respectively of the IGBT module. The conduction loss of switches $S_{A1} - S_{C2}$ are given as-

$$P_{C_{S_X}} = \frac{m V_{CE,S_X,1,2} I_{pk}}{4n} + \frac{2n}{3 \pi n^2} R_{CE,S_X,1,2} I_{pk}^2$$

(17)

Where $X \in \{A, B, C\}$ and $V_{CE,S_X,1,2}$ and $R_{CE,S_X,1,2}$ are constant voltage drop (1.4V) and on state resistance (22mΩ) of IGBT modules used for $S_{X1} - S_{X2}$. The conduction loss expression of anti-parallel diodes of switch pairs $S_{X1} - S_{X2}$ is given in (18).

$$P_{C_{D,S_X}} = \frac{V_{D,X,1,2} I_{pk}}{\pi n} + \frac{R_{D,X,1,2} I_{pk}^2}{4n^2} - \frac{mV_{D,X,1,2} I_{pk}^2}{4n} - \frac{mR_{D,X,1,2} I_{pk}^2}{1.5 \pi n^2}$$

(18)

The anti-parallel diodes have a voltage drop $V_{D,X,1,2}$ (1.1V) and on state resistance $R_{D,X,1,2}$ (18mΩ). The conduction losses in a secondary diode of $D_{a1} - D_{c4}$ and a IGBT switch of $Q_{a1} - Q_{c2}$ are given in (19).

$$P_{C_{D_{a1}}} = \frac{V_{D_{a1}} I_{pk}}{2 \pi} + \frac{R_{D_{a1}} I_{pk}^2}{8}$$

(19)

$$P_{C_{Q_{a1}}} = \frac{V_{CE_{a1}} I_{pk}}{\pi} + \frac{R_{CE_{a1}} I_{pk}^2}{4}$$

$V_{D_{a1}}$ (1.16V), $V_{CE_{a1}}$ (1.48V) and $R_{D_{a1}}$ (4mΩ), $R_{CE_{a1}}$ (2.3mΩ) are the constant voltage drop and on state resistance of the secondary diode $D_{a1}$ and IGBT $Q_{a1}$ respectively. In Fig. 17, the pole current envelopes of $S_{A1} - S_{A2}$ ($I_{pa_a}$) and $S_1 - S_2$ ($I_{pa_s}$) are shown. $S_1 - S_2$ is completely soft-switched. In Fig. 17, the shaded portions in $I_{pa_a}$ indicate hard-switching zones of $S_{A1} - S_{A2}$. The range of soft turn ON of $S_{A1} - S_{A2}$ is given as ($\theta_1, \pi - \theta_1$), as shown in Fig. 17. $\theta_1$ is given in (20).

$$\theta_1 = \sin^{-1} \left( \frac{2nC_I V_{dc}}{I_{pk} DT_a} \right)$$

(20)

$DT_a$ is the dead time between the gating pulses of $S_{A1} - S_{A2}$. Switching loss of $S_{A1}$ is given in (21).

$$P_{S_{A1}} = \frac{2V_{dc} I_{pk}}{n \pi T_s} \left( \frac{E_{ONR} + E_{OFFR}}{V_{CCI}} \right) (1 - \cos \theta_1)$$

(21)

$E_{ONR}$ and $E_{OFFR}$ are the turn ON and OFF energy losses at rated condition ($V_{CCI}, I_{C}$) given in device datasheet.

B. Power loss in HFTs

Copper loss of a HFT can be given as- $P_{cu,HFT} = \frac{I_{pk}^2}{2} \left( \frac{R_{AC,p}}{n^2} + R_{AC,s} \right)$, where $R_{AC,p}$ and $R_{AC,s}$ are primary and secondary winding AC resistances of the HFT. The core loss of the HFT is estimated at peak operating flux density using core loss per unit volume versus operating frequency plot provided in the core datasheet.

C. Experimentally measured loss

The converter power loss is measured experimentally using Vitrek precision multi-channel harmonic power analyser PA300 by taking the difference of measured power between input and output of each stage. Table II summarises the input quantities (voltages and currents) to the VA300 to measure power at different stages of the proposed inverter. In Fig. 2a, measured voltages, currents and powers in different stages are indicated. The DC side converter loss is measured as $(P_{in} - P_{out,dc})$. In similar way, the loss in each stage of the converter is measured experimentally.

---

**Fig. 27.** (a) Efficiency of the proposed HFL inverter, (b) Power loss at different stages of $3\phi$ HFL inverter

**Fig. 28.** (a) Power loss break down at 3.94kW output power obtained experimentally and analytically, (b) Percentage loss distribution shown at 3.94kW output power obtained experimentally, (c) Percentage loss distribution in the DC side converter shown at 4kW output power obtained analytically (SL-switching loss, CL- conduction loss)

Fig. 27a presents the converter efficiency for a variation of load from 1kW to 4kW with input DC supply 350V. The converter has a peak efficiency of 91.6% at 2.2kW load.
In Fig. 27b the variation of power losses in different stages of the converter are plotted against the load variation. Among different stages the high frequency switched primary bridge incurs maximum loss. The loss is reduced with the increase of load as the soft-switching zone is increased. Loss contributed by the line frequency switched secondary converter is relatively less (around 1%). This result shows the effectiveness of the line frequency switching based modulation strategy.

Fig. 28a shows power loss distribution for 3.94kW load obtained experimentally and analytically. The analytically estimated losses are closely matching with the experimentally obtained values other than the DC bridge. A 15% difference is observed in experimental and analytical obtained loss of the DC bridge. This difference is mainly the due to variation of device on state resistance with temperature and inaccuracy in estimation of hard-switching zone of $S_{A1} - S_{C2}$.

Fig. 28b presents a pie chart showing experimentally obtained losses at 3.94kW output power. The primary bridge incurs 57% loss compared with 14% of the secondary converter.

In Fig. 28c, the pie chart shows analytically obtained DC side converter loss distribution at 3.94kW output power. The conduction loss (CL) in $S_1 - S_2$ dominates the loss. As $S_{A1} - S_{C1}$ are partially soft-switched, they also have switching loss (SL).

Fig. 29 presents the primary bridge loss variation over the load range. Experimental and analytical loss of the soft-switched primary bridge is presented along with complete hard-switched loss of the primary bridge. The soft-switching of the primary bridge significantly reduces the converter loss at high output power (as $\theta_1$ is reduced in Fig. 17).

In Fig. 30, experimentally measured THD of output pole voltage ($v_{ang}$) and line current are shown. The pole voltage has a THD of 69% with an effective modulation index 0.8. As seen from Fig. 30a, after fundamental most dominant frequency components are at 40kHz which is twice of the DC bridge switching frequency. The line current THD is 5.1%.

VI. COMPARISON WITH OTHER TOPOLOGIES

In this section a detailed comparison of the proposed solution is presented with a) topology 1- a ZVS phase-shifted full-bridge (PSFB) DC-DC converter followed by a $3\phi$ voltage source inverter (in Fig 31a) and b) topology 2- a ZVS PSFB DC-DC converter followed by a quasi-resonant DC link inverter (QRDCL). In the second topology a resonating cell with three active switches (Fig. 31b) is connected between the PSFB and $3\phi$ VSI (Fig 31a) to achieve ZVS of the $3\phi$ VSI. The QRDCL circuit is shown in Fig. 31b [17]. The comparison is shown for a target application of grid integration of utility scale photovoltaic system with the specification given in Table III.

The proposed inverter is modulated at a modulation index $m = 0.85 = \frac{nV_{pk}}{V_{dc}}$. Thus the high frequency transformer (HFT) primary to secondary turns ratio, $n = 2$. IGBT SKM450GB12T4 (1200V,450A) are considered for the DC side switches $S_1 - S_2$ and the AC side switches $Q_{a1} - Q_{c2}$.

---

**TABLE II**

<table>
<thead>
<tr>
<th>Inputs to PA300</th>
<th>$V_{dc}$</th>
<th>$I_{dc}$</th>
<th>$V_{a,b,c}$</th>
<th>$I_{a,b,c}$</th>
<th>$P_{in}$</th>
<th>$P_{out,dc}$</th>
<th>$P_{out,HFT}$</th>
<th>$P_{out,AC}$</th>
<th>$P$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured power</td>
<td>$P_{in}$</td>
<td>$P_{out,dc}$</td>
<td>$P_{out,HFT}$</td>
<td>$P_{out,AC}$</td>
<td>$P$</td>
<td></td>
<td></td>
<td></td>
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</tr>
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</table>

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TABLE III
TARGET DESIGN SPECIFICATION

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power (P)</td>
<td>200 kW</td>
</tr>
<tr>
<td>Input DC (Vdc)</td>
<td>800V</td>
</tr>
<tr>
<td>Output phase AC peak (Vpk)</td>
<td>339V (415V L-L RMS)</td>
</tr>
<tr>
<td>Switching frequency (fsw)</td>
<td>20kHz</td>
</tr>
<tr>
<td>Line frequency (fl)</td>
<td>50Hz</td>
</tr>
</tbody>
</table>

Fig. 31. (a) Topology 1: PSFB+3φ VSI, (b) Circuit diagram of QRDCL [17]

The switches $S_{A1} - S_{C2}$ are implemented with IGBT SKM400GB125D (1200V,300A) whereas MEO 450-12DA (1200V,450A) is considered for secondary diodes $D_{a1} - D_{c3}$.

To be consistent, the DC-DC and the three-phase inverter in both topology 1 and 2 are modulated near the 85% of their respective maximum voltage transfer ratio. The DC-DC converter is modulated as PSFB [34] with duty ratio $D = 0.85 = \frac{nV_{in}}{V_{dc}}$ whereas the inverter is modulated with conventional space vector PWM with modulation index $M = 0.864 = \sqrt{3} \frac{V_{pk}}{V_{in}}$. This implies $V_{in} = 680V$, (see Fig. 31a) and HFT turns ratio $n = 1$. In topology 1, all active switches in PSFB and 3φ VSI are implemented using IGBT SKM450GB12T4. MEO 450-12DA is considered for the PSFB diode bridge.

The PSFB and the 3φ VSI in topology 2 are same as in topology 1. The QRDCL is designed based on the procedure given in [17]. $S_{R1}$ is implemented with IGBT FZ1200R12HP4 (1200V, 1200A). IGBT FZ600R17KE3 (1700V, 840A) is used for $S_{R2}$. 1200V, 900A IGBT SKM900GA12E4 are used for $S_{R(3,4)}$.

Table IV summarises the comparison in terms of number of passive and active semiconductors, their blocking voltage $(V_b)$, peak $(I_P)$ and RMS $(I_{RMS})$ current. S.F is the scaling factor. The proposed topology uses 8 active switches in the DC side converter where the RMS current of 6 switches are 2.3-2.5 times less than the 4 DC side switches of the topology 1 and 2. The RMS current of the remaining two switches are slightly more. Blocking voltage of the devices are same as input DC bus voltage $V_{dc}$ in all three topologies.

In the AC side, the proposed topology and the topology 1 have 6 active switches with similar RMS current and blocking voltage. The topology 2 needs 3 additional switches with high voltage and current stress to implement QRDCL. The blocking voltage of $S_{R2}$ is 4.4 times the peak output voltage $(V_{pk})$. The current stress of all three switches are high and is maximum for $S_{R1}$, approximately 2.9 times the 3φ VSI switches. The RMS current rating of $S_{R1}$ is approximately 1.7 times higher than the 3φ VSI switches. This results in significant additional conduction loss added to the AC side of the converter causing further decrease in converter efficiency. Now the 3φ VSI is soft-switched at the expense of additional active switches with very high voltage and current stresses. The proposed topology uses 12 diodes with same blocking voltage and 60% RMS current of the topology 1 and 2 that use 4 diodes in the AC side.

Loss and efficiency of the three topologies are presented in Table V where $P_{CL}$ and $P_{SL}$ are the conduction and switching loss respectively. The efficiency does not include the losses in HFTs and filters. The conduction loss in DC side converter of the proposed topology is slightly higher than the topology 1 and 2. The switching loss in DC side converter is negligible due to zero voltage switching (ZVS) in all three solutions. In the AC side, the topology 2 has higher conduction loss than other two topologies. The topology 1 has high switching loss due to hard-switching of the AC side 3φ VSI. As the

![Diagram of topology 1: PSFB+3φ VSI](image-url)

![Diagram of QRDCL circuit](image-url)

![Comparison table](chart-url)
AC side switches in the proposed solution and topology 2 incur negligible switching loss, they achieve similar efficiency. But in topology 2, this improved efficiency comes at the cost of using higher rated active devices in QRDCL cell. The decoupling of switching frequency with the losses in the proposed solution, provides an opportunity to push for higher switching frequency and hence smaller size of the filters and cost.

The proposed topology employs three HFTs where the secondary has two identical windings. The topology 1 and 2 use a single two-winding transformer. As the power flow in the proposed topology gets divided into three high frequency transformers, the RMS winding currents and individual area product are significantly small when compare with the topology 1 and 2 (see Table VI). But due to push-pull winding structure of the secondary windings, the total area product for the proposed solution is 1.7 times, that of the conventional one.

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### Table V
Loss Comparison (Scaling Factor \( \frac{P_{\text{L}}}{V_{\text{dc}}} \))

<table>
<thead>
<tr>
<th></th>
<th>Topology 1</th>
<th>Topology 2</th>
<th>Proposed topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC side</td>
<td>( P_{\text{L}} ) 0.445</td>
<td>0.445</td>
<td>0.7</td>
</tr>
<tr>
<td>AC side</td>
<td>( P_{\text{L}} ) 1.03</td>
<td>1.23</td>
<td>1.138</td>
</tr>
<tr>
<td>Total Loss</td>
<td>( P_{\text{T,L}} ) 2.353</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Efficiency</td>
<td>( \eta ) 96.3</td>
<td>98.35</td>
<td>98.2</td>
</tr>
</tbody>
</table>

### Table VI
High Frequency Transformer Comparison

<table>
<thead>
<tr>
<th></th>
<th>S.F.</th>
<th>Topology 1&amp;2</th>
<th>Proposed topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{RMS, pri}} )</td>
<td>( \frac{p}{V_{\text{dc}}} )</td>
<td>1.33</td>
<td>0.557</td>
</tr>
<tr>
<td>( I_{\text{RMS, sec}} )</td>
<td>( \frac{p}{V_{\text{pk}}} )</td>
<td>0.565</td>
<td>0.334</td>
</tr>
<tr>
<td>Area product</td>
<td>( \frac{p}{V_{\text{pk}}\cdot V_{\text{dc}}} )</td>
<td>0.425</td>
<td>0.242</td>
</tr>
<tr>
<td>HFT count</td>
<td>–</td>
<td>1</td>
<td>3</td>
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### Table VII
Filter Size Comparison Using THD

<table>
<thead>
<tr>
<th></th>
<th>Topology 1&amp;2</th>
<th>Proposed topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Side</td>
<td>( 0.42 ) (( THD_{1} ))</td>
<td>0.55 (( THD_{1} ))</td>
</tr>
<tr>
<td>AC Side</td>
<td>( 0.69 ) (( THD_{1} ))</td>
<td>( 0.6 ) (( THD_{1} ))</td>
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<tr>
<td>Intermediate</td>
<td>( 0.42 ) (( THD_{1} ))</td>
<td>0.48 (( PSFB ))</td>
</tr>
<tr>
<td>DC Link</td>
<td>( 0.42 ) (( THD_{1} ))</td>
<td>( 3\sigma ) (( VSI ))</td>
</tr>
</tbody>
</table>

Filter requirement comparison

The filtering requirement can be expressed in terms of voltage and current THD [35]. In Table VII, the filtering requirements are compared between the proposed topology and topology 1 and 2 for the target specification. The topology 1 and 2 require additional filter after the DC-DC stage. For which both the capacitive and inductive filter requirement in topology 1 and 2 are 1.5-2 times when compared with the proposed solution. Hence, from the filter requirement perspective, the proposed solution is cost effective and will result in higher power density. Moreover, in any multi-stage solution, some additional capacitance (over and above than what is required for filtering) are used in the DC link to support load transient. Hence, an electrolytic capacitor is mostly employed and which is considered to be the most unreliable component. One of the major objective of proposed single stage configuration is the elimination of this capacitance.

### VII. Conclusion

This paper presents a single-stage high frequency link converter topology that supports active power transfer from DC to AC at near UPF condition. A 4kW laboratory scale hardware prototype is built and tested. The suggested sine PWM based modulation strategy results in high quality output, evident from the AC side line currents obtained experimentally. This technique also ensures line frequency switching of the AC side converter incurring negligible switching loss. The converter loss is analytically estimated and the estimation is experimentally verified. The experimentally obtained loss breakdown verifies high efficiency of the secondary converter. Zero voltage switching (ZVS) of all active devices in the DC side converter with the help of circuit parasitics has been analysed and experimentally verified. The soft-switching of the primary side converter significantly reduces the converter loss at high power. The proposed converter with high frequency galvanic isolation provides a compact, cost effective and efficient solution for the utility scale grid integration of renewables.

### References

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics


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