An accurate CV-CC Non-isolated Buck Battery Charger Using Primary side PWM Controller

Baiju Payyappilly
Power Systems Group
ISRO Satellite Centre
Bangalore-560017, INDIA
Email: bbp@isac.gov.in

Vinod John
Department of Electrical Engineering
Indian Institute of Science
Bangalore-560012, INDIA
Email: vjohn@ee.iisc.ernet.in

Abstract—Primary side flyback PWM controllers are available with large number of protection features such as over current protection, over/under input voltage protection, over output voltage protection etc., and designs using such controllers can be cost effective. They are designed for flyback dc-dc converters for low power CV-CC applications like LED lighting and mobile/PDA battery chargers. Using this type of controllers for a Buck type CV-CC battery charger, which can be designed for higher power levels is a low cost option. It offers accurate CV-CC control function with a stable change over between constant current and constant voltage regimes. It is shown that the resulting design can fully utilize the protection features, which increases safety and reliability. This paper presents the design of a 14V, 7W CV-CC battery charger using such an integrated controller and explains the modifications required for the flyback controller to work as a buck CV-CC charger.

I. INTRODUCTION

High accuracy constant current/ constant voltage (CC-CV) battery chargers are necessary for characterization and modeling of batteries. Especially the Li-ion batteries, which are the popular ones presently, demands very accurate current and voltage settings due to the nature of its electro chemistry. Also they are very sensitive to over charge, which can result in fire hazards.

To efficiently charge a Li-ion battery, the popular method used is CC-CV technique. There are three distinct phases for a CC-CV controller. Constant current phase, change over phase from CC to CV and constant voltage phase. Smooth and safe change over from CC to CV is critical to the charger [2].

Many techniques have been proposed to implement this two loop control. Jung et al. [3] uses a p-n-p transistor to switch between the two control loops, Tsai et al. [4] switch between two separate low drop out regulators (LDO) to implement the loop change over, and Liu et al. [5] uses Field Programmable Gate Arrays (FPGA) and micro controllers for the same change over. Chen et al. [2] uses a diode for transition between two high gain linear feedback loops (voltage and current loops), and controls a single MOS device to achieve CV-CC charging. However, this being a linear regulator, there is always power loss in the series device while charging.

Many PWM controllers are available today for primary side feedback control of flyback dc-dc converter at low cost and having low power consumption. One such controller, R7710[1] is designed to regulate the output voltage or current accurately, by sensing an auxiliary output voltage and primary current.

A buck non-isolated power converter is controlled using the above mentioned controller, so that the design can be extended to high power levels. The proposed design provides the advantages of, accurate current regulation for the entire dc input voltage range for the design, smooth and stable transition from CC to CV and utilizes a small 6 pin package controller.

II. DESIGN OF THE BUCK CHARGER

Circuit implementation of the proposed CV-CC charger is shown the schematic diagram in Fig.1. The six pin chip $U_1$ is the primary side controller. The start-up power for the controller is provided by the series regulator, which is identified in Fig.1. This series regulator provides 18V to the controller. The auxiliary flyback converter is formed by Mosfet $M_1$, flyback inductor $T_{X_1}$, diode $D_7$ and associated components. The output of the flyback converter is OR’ed with the start-up regulator output.

Mosfets $M_2$ and $M_3$, inductor $L_1$ and Capacitor $C_5$ constitute the non-isolated buck converter, whose output is regulated by the feedback to the controller. A PNP transistor $Q_2$ is used for multiplexing the output voltage feedback from buck converter and secondary voltage from flyback inductor to the pin-4 of the controller($U_1$). Multiplexing is controlled using the gate drive signal from pin-1 of the controller, which also drives the flyback switch($M_1$) as well as buck switches($M_2$, $M_3$).

A resistive current sensor ($R_{S}$) is used as shown in the schematic in Fig.1, to provide current feedback to the controller. The resistive dividers $R_{14}$ and $R_{15}$ provides a means for fine tuning the limiting current.

A. Sensing of Input and Output Voltages

The sensing of input voltage, output voltage and compensation for cable drop in output line are achieved through the single pin (pin-4,voltage sense pin) of the controller.

To retain the utilization of the features in the controller, one has to have a flyback converter which provides an auxiliary output. Hence the design has to have an embedded flyback part. For the main power flow to the battery, the buck stage is
proposed in addition to the auxiliary flyback stage. The gate drive signal is used for driving the power switch (MOSFET) of the buck stage, in addition to the driving of flyback switch. The feedback loop for regulation of voltage and current is from this buck stage.

Hence, the overall design has a single controller, which drives a buck stage and an auxiliary flyback stage simultaneously. Output voltage or current is regulated for the buck stage alone and flyback output is in open loop. The flyback output is sensed for implementing input over voltage or under voltage protection as well as it powers the controller when the nominal dc input voltage is above 40V.

The output feedback voltage sense pin (pin-4) of the controller has multiple functions. It serves functions of output voltage sense and input voltage sense. The output voltage sense is done during the OFF time of switch gate drive. While the input voltage sense is done during the ON time of gate drive pulse. This is achieved by sensing the auxiliary flyback secondary voltage during ON period of the gate drive pulse, and sourcing a current ($I_{clamp}$) from the pin-4 to clamp this negative voltage to zero. The internally sourced current, $I_{clamp}$ needed for clamping is a measure of input voltage.

To facilitate for the multiple function of the voltage sense pin, it needs to be connected to the buck stage output voltage sense, during the OFF time of the gate drive signal, and connected to flyback auxiliary output sense, during the ON time. This is achieved by de-multiplexing this pin using a PNP transistor ($Q_2$), diode ($D_5$) and driving the transistor from gate drive signal, as shown in Fig. 2(a). During the ON time PNP transistor $Q_2$ is OFF and hence the pin4, get connected to $V_{AUX}$ sense line. This is a negative voltage proportional to the negative $V_{in}$ of the flyback converter, when the flyback transistor M1 is ON. The internal current source clamps this voltage to zero and thus senses the input voltage. During OFF time as $Q_2$ is ON, the pin4 gets connected to buck output voltage sense line, and during this time $V_{AUX}$ is positive and is blocked by by $D_5$. The sensed voltage is used for deciding the duty cycle of the gate drive pulse.

**B. Input Over Voltage Limit**

The $I_{clamp}$ sourced from the Pin-4 of the controller (Fig. 2(a)) during ON time is proportional to $V_{in}$ and has a maximum limiting value of 1.5 mA. Beyond this limit the controller is shut downed.

$R_{FB2}$ is selected to get $I_{clamp}$ of 1.5mA at the maximum input voltage. Now, the resistor value for $R_{FB1}$ is selected to set the buck sense voltage=2.5V, during the constant voltage regime. This is set for an output voltage of 14.2V.

$$R_{FB2} = \frac{V_{IN(max)} N_{AUX}}{1.5 N_P}$$

$$14.2 \times \frac{R_{FB1}}{R_{FB1} + R_{FB2}} = 2.5$$

**C. Input Under Voltage Limit**

The nominal working supply voltage range of the controller is 16V to 27.5V. The start up series regulator is set at 18V and powers the controller from the DC bus. The start up regulator
output and $V_{AUX}$ are ORed. Whenever $V_{AUX} \geq 18V$, the controller gets powered from $V_{AUX}$. With reduction in $V_{IN}$, $V_{AUX}$ increases as,

$$V_{AUX} = \frac{N_{AUX}}{N_p} \times \frac{D}{1-D} \times V_{IN} \quad (3)$$

where D is the duty cycle of switch. D is decided by the $V_{IN}$, as the buck output ($V_{OUT}$) is regulated. Whenever $V_{AUX} \geq 27.5V$, controller shuts down the PWM.

With this design feature, input under voltage limit can be set by selecting the $\frac{N_{AUX}}{N_p}$ turns ratio to make $V_{AUX} = 27.5V$ at the minimum input voltage expected ($V_{IN(\text{min})}$).

$$\frac{N_{AUX}}{N_p} = \frac{27.5}{V_{IN(\text{min})}} \times \frac{1-D_{\text{max}}}{D_{\text{max}}} \quad (4)$$

Where, $D_{\text{max}}$ is the duty cycle at $V_{IN(\text{min})}$.

D. Current Sensing

The buck stage output need to be in CV-CC mode. For this output current for buck stage to be sensed and fed to the controller. In this work, a resistive current sensor is used as shown in Fig. 1. The controller design is for a low side resistive current sensor in the primary side of flyback converter. Hence the location of the sensing resistor is chosen, so that the current through the sense resistor is same as that flows through transistor M2, which resembles the flyback primary side current.

The current proportional voltage fed to the current sense pin of the controller, need to be confined to a value, which is less than 1.7V. For this, as well as to have a provision to adjust the constant current(CC) limit, the output of sensor is scaled using $R_{15}$ and $R_{14}$ combination as shown in Fig. 2(b). By varying $R_{15}$, the CC limit can be set.

The controller samples the current proportional voltage($V_{CS}$), at the end of the ON period of transistor M2. There is an internally set limit on the product of OFF time of M2 and the sampled current proportional voltage, which is $\approx 7.5\mu V.s$.

The scaling of the sensor output is done such that, for the intended limiting ranges of output current, the product of scaled current sensor output ($V_{CS}$) and OFF time of the switch $M2$ ($t_{OFF}$) gives $\approx 7.5\mu V.s$.

The output current in a buck converter working in the boundary of continuous mode is given by,

$$I_o = I_{M2-pk} \times \frac{t_{OFF}}{T} \times 0.5 \quad (5)$$

$$I_o \propto I_{M2-pk} \times t_{OFF} \quad (6)$$

$$I_o \propto (V_{CS} \times t_{OFF}) \quad (7)$$

Where,

$I_o$ = output current

$I_{M2-pk}$ = Buck switch (M2) current.

This has the effect of constant charge flow (current x time) for each cycle, and amounts to constant current flow as period (T) is fixed. This implementation is helpful in maintaining accurate constant current, for all duty cycle conditions. The CV-CC control characteristic of the controller is shown in Fig. 2(c). The figure shows plot of output voltage versus peak of sensed current at pin-6 of the controller. The values of $R_{15}$ and $R_{14}$ are selected to give the required $I_{M2-\text{limit}}$.

$$I_{M2-\text{limit}} = \frac{7.5}{R_{S}\cdot(\frac{R_{15}}{R_{14}+R_{15}})\cdot t_{off}} \quad (8)$$

where, $R_{S}$ is the current sense resistor value in $\Omega$ and $T_{off}$ (in $\mu$s) is the OFF time of the transistor $M2$.

E. Snubber Design

The PWM controller used has a burst frequency control, which results in spreading of the switching noise spectrum to meet the EMI/EMC standards.

Apart from EMI improvement, snubber is necessary in primary and secondary sides of flyback auxiliary output, to prevent,

- Avalanche break down of the MOSFET (M1)
Core loss for 1A ripple: 406mW
270mW
Resistive
280mW
26mW
470mW
850mW
IRF 840(500V, 8Amp)

The frequency of operation is optimized for reduction in isolated converter, is designed for a maximum ripple current

The ringing frequency \( f_r \) is around 2MHz and assuming a leakage inductance \( L_1 \) in the range of 50 - 100 \( \mu \)H, the snubber resistor \( R \) can be chosen as equal to the characteristic impedance of the resonant circuit[6]. Snubber Capacitor \( C \) is chosen such that, its impedance is equal to \( R \) at the resonant frequency \( f_r \). For the selected values of snubber resistor and capacitor (150\( \Omega \) and 330pF respectively), the snubber dissipation is \( \approx 28 \) mW, at an input voltage of 50V.

2) Primary Snubber: The primary snubber used is a series combination of a zener diode and a diode across the primary winding (Fig. 1). The power rating of the zener diode is arrived at based on the maximum stored energy in leakage inductance of the flyback converter.

The rise in switching loss with frequency, and hyperbolic reduction of inductor losses[7] (for \( \approx 24^\circ \)C temperature rise in inductor and 1A peak to peak ripple current) at the same time, are considered to arrive at the optimum switching frequency. This is found to be around 40kHz. The designed elements for the buck stage are listed in Table 1.

### III. Experimental Results

The circuit schematic of the implementation is as shown in Fig. 1. The buck power stage was set for a constant current level of 300mA, and constant voltage level of 13V. The characteristics is measured using a 50\( \Omega \) rheostat as load, instead of battery. The input DC bus was provided by Agilent make DC power supply. The DC bus capacitor used is 470\( \mu \)F. The output filter capacitor for buck stage also was of same value.

The drain voltage of flyback MOSFET \( M_1 \) and sensed drain current of buck MOSFET \( M_2 \), at pin-6 of controller \( U_1 \) are shown in Fig. 4(a) and Fig. 4(b) along with the drive signal from the controller.

The losses in the implementation are contributed from the load on auxiliary flyback output, losses in flyback and buck converter switches and buck stage inductor. An estimation of various component losses for a CC limit of 300mA and CV limit of 13V are tabulated in Table 2. From this data the estimated efficiency when the charger is operating at the boundary of CC and CV regimes, is 68.9%.

The measured overall efficiency of the buck charger for a nominal input voltage of 42V and output load current of 300mA at 13V output voltage is 64%. The efficiency calculation does not include the losses in the isolated gate drive circuit, which was powered from a stand alone power supply.

### A. Transient Response

The transient behavior of the design for a sudden change in load current, where it changes over from CV mode to CC mode and vice versa are shown in Fig. 5. Equivalent circuit of the system during the transients is shown in Fig. 3. The behavior for a CV to CC transient is a first order one. But, the

---

**Table I. Components in Buck Converter**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor</td>
<td>240µH (Ferrite toroidal core)</td>
</tr>
<tr>
<td>Core loss for 1A ripple</td>
<td>406mW</td>
</tr>
<tr>
<td>Copper Loss for 6A</td>
<td>2.976W</td>
</tr>
<tr>
<td>MOSFET</td>
<td>IRF 840(500V, 8Amp)</td>
</tr>
<tr>
<td>Filter Capacitor</td>
<td>470µF</td>
</tr>
<tr>
<td>Current sensor</td>
<td>Resistive 1Ω</td>
</tr>
</tbody>
</table>

**Table II. Estimate of Dissipation in Components**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor and Ohmic</td>
<td>270mW</td>
</tr>
<tr>
<td>Buck MOSFET(( M_2 ))</td>
<td>280mW</td>
</tr>
<tr>
<td>Buck MOSFET(( M_3 ))</td>
<td>45mW</td>
</tr>
<tr>
<td>Flyback MOSFET(( M_1 ))</td>
<td>285mW</td>
</tr>
<tr>
<td>Current sensor</td>
<td>26mW</td>
</tr>
<tr>
<td>Load on flyback stage</td>
<td>850mW</td>
</tr>
</tbody>
</table>

---

![Fig. 3. Equivalent circuit to model the transient response](image-url)
Vgs
Vds
(a)

Fig. 4. Experimental waveforms (a) Gate to source voltage ($V_{gs}$) and drain voltage ($V_{ds}$) of M1 (b) Gate to source voltage ($V_{gs}$) and sensed drain current ($I_d$) of M2

Vgs
I d
(b)

I out
Vout
(a) CV to CC transient with low CV load current of 280mA

I out
Vout
(b) CC to CV transient with low CV load current of 280mA

I out
Vout
(c) CV to CC transient with high CV load current of 400mA

I out
Vout
(d) CC to CV transient with high CV load current of 400mA

Fig. 5. Transient responses for transition between CC and CV modes ($I_{out}$: 200mA/Div)

CC to CV transient results in a second order response of the form,

$$V_{\delta}(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$  \hspace{1cm} (10)

where, $\omega_n = \frac{1}{\sqrt{L_1C_5}}$ is the resonant frequency of output side in radians/s. and $\zeta = \frac{L_1}{L_1C_5} \cdot \frac{1}{2R_L}$ is the damping factor. $V_{\delta}$ is the impulse voltage function representing the additional energy to be dissipated for achieving the steady state. Since the damping factor depends on the output current during CV mode, the CC to CV response depends on the CV mode load current. The response in Fig. 5(b) is for 280mA load current and that in Fig. 5(d) is for 400mA load current.

The implementation was tested for CC-CV charging of a three series cell battery, made using LG make 2.5 Ah, Li-ion cells. The CC limit was set for 300mA and CV limit at 12.4V. The battery voltage and current waveforms during the charging is shown in Fig. 6. The photograph of the test set-up is shown in Fig. 7.

IV. CONCLUSION

The design and implementation of non-isolated buck type accurate CC-CV Li-ion battery charger having strong protection features like input and output over voltage/ under voltage protection, output short circuit protection and thermal shut down is carried out in this work. The design is carried out using a flyback primary side PWM controller.
Fig. 6. Experimental waveforms during CV-CC charging of Li-ion battery (a) Battery terminal voltage (b) Battery charging current

Fig. 7. Photograph of the test set-up

Modifications needed to implement a buck CV-CC battery charger utilizing flyback primary side controller is explained.

The design provides a smooth transition between constant current and constant voltage control loops and accurate constant current regime.

The prototype is tested for a constant current level of 300mA, and constant voltage level of 12.2V, to charge a Battery pack of three series connected LG make Li-ion 2.5Ah cells. It can be upgraded to higher power levels.

References