Abstract—Widely distributed single-phase power electronic rectifier loads are an increasing source of harmonics in the power distribution system. These harmonics have many well-known adverse impacts on the power system, so it is necessary to improve the power quality of the rectifiers. This paper presents a novel single-phase rectifier in which capacitors are used in parallel with diodes in one leg of the rectifier. A general analytical model of the proposed topology is obtained. The closed-form expressions for the rectifier waveforms are utilized in parameter selection that leads to optimal performance in terms of input current total harmonic distortion (THD). Different topologies of rectifiers are compared in terms of the input voltage, current waveform distortion, output dc voltage ripple, and desired target for the dc output voltage. The proposed topology reduces the THD from 145% in a normal rectifier to 63% while maintaining voltage ripple less than 0.3%. The proposed topology keeps dc bus ripple small while simultaneously providing better THD. The passive components considered for improving harmonic injection are two small capacitors. The additional cost required for the proposed rectifier is low, and the proposed rectifier also has a higher efficiency than the other commonly used diode rectifier topologies.

Index Terms—AC–DC power conversion, capacitive filter, diode bridge rectifier, line-current total harmonic distortion (THD), naturally commutated rectifier, split-capacitor full-bridge (SCFB) rectifier.

I. INTRODUCTION

NONLINEAR loads such as controlled and uncontrolled, single-phase, and three-phase rectifiers inject considerable amount of lower order harmonics into the grid and distorts the voltage at point of common coupling [1], [2]. Harmonics cause excessive heating, pulsating, and reduced torque in motors and generators, increased heating and voltage stresses in capacitor, malfunction of switch gears, and relays and reduces the life of products [3], [4]. It is, therefore, necessary to reduce harmonics in the electric power system. Also, in case of dc loads, it is important to get low ripple in the output dc voltage for its proper functioning [5]. So, it is necessary to provide dc output at low ripple keeping the harmonics injected in the line to a reasonable low value.

Passive front-end (PFE) rectifiers followed by power factor correction (PFC) stage, and active front-end (AFE) rectifiers maintain dc bus voltage at desired level and harmonics injected, at switching frequency, can be filtered out using first-order filters [6]–[8]. Using the aforementioned topologies, for low power applications such as light-emitting diode (LED) lighting, increases the cost as it requires active switches such as MOSFET or insulated gate bipolar transistor (IGBT) and additional sensors, for controlling the dc bus voltage and input current [9]. So, for lower power applications, PFE rectifier circuits, diode rectifier with a capacitive filter, as shown in Fig. 1(a), and voltage doubler rectifier with two split capacitances, as shown in Fig. 1(b), are preferred. It is well known that a diode rectifier with a capacitive filter, as shown in Fig. 1(a), has a negligible output voltage ripple but injects significant amount of lower order harmonics into the grid. Voltage doubler, shown in Fig. 1(b), has low harmonic injection if $C_s$ is kept small but ripple in the output voltage is considerably high.

According to IEC 61000-3-2, equipments are classified in four categories, Class A, Class B, Class C, and Class D.
Lighting equipments, whose front end is a rectifier, fall into Class C and harmonic standards for these equipments are summarized in Table I. In this paper, a new split capacitor full-bridge (SCFB) rectifier is proposed [10]. The proposed SCFB rectifier shown in Fig. 1(c) is suited for low power applications. An SCFB rectifier is a combination of the diode rectifier with a capacitive filter and voltage doubler topology. Initial simulation studies comparing the three topologies shown in Fig. 1 is summarized in Section II. The analytical closed-form expressions for waveforms are covered in Section III and Appendix. The equations for waveforms of the SCFB rectifier that are derived in this paper are used for circuit optimization. This leads to circuit parameters that meet tight dc voltage ripple requirement while simultaneously having minimum input current distortion. Section IV details analytical, simulation, and experimental results. This section also covers the effects of line inductance and load capacitance in the optimal values split capacitor, and total harmonic distortion (THD) of the line current drawn. A simplified approach, based on power balance, for the design of a split capacitor is discussed in Section V. Section VI concludes this paper.

II. SIMULATION STUDIES

Initial simulations on all three topologies, shown in Fig. 1 were carried to check the performance of the proposed model. Per unit values and design specifications of the converter used for simulation are given in Table II(a) and (b), respectively. $P_o$, $V_g$, $f_s$ = 50 Hz, $R_L$, $L_g$, and $R_g$ are rated power, grid voltage RMS, grid frequency, line impedance, and load resistance, respectively. With line impedance neglected, effects of variations in values of load capacitance, $C_L$, and split capacitance, $C_s$, in grid current THD and ripple in the output voltage are studied. Summary of the results in tabulated in Table III. It can be observed that the proposed SCFB topology has the advantages of both the normal rectifier with low output voltage ripple, and voltage doubler circuit with lesser distortion in the line current drawn.

III. ANALYSIS OF THE SCFB RECTIFIER

Fig. 2 shows the split-capacitor full-bridge (SCFB) rectifier and its operating modes. The grid is modeled as a sinusoidal voltage source $v_g$ in series with line impedance consisting of $R_g$ and $L$ in series. The load is modeled as a resistor ($R_L$). For modeling of the topology, different modes of operation are identified and the governing equations of these modes are covered in this section. The analysis is carried out for positive half cycle of $v_g$. Conducting elements of in each mode are shown as dark black shade and the nonconducting elements are in light black shades, as shown in Fig. 2. The main assumptions for this analysis are as follows.

1. Diodes are assumed ideal.
2. ESR of the capacitors have been ignored.
3. Ratio $\Delta V_o/V_o \ll 1$.

A. Mode-I From $t_1 < t < t_2$

In Mode-I, during the positive half cycle of the grid supply diode $D_1$ starts conducting, at $t = t_1$. At $t = t_1$, $v_{c1}(t_1) = V_1 = V_g(t_1)$, $v_{c2}(t_1) = V_2$, $i_L(t_1) = 0$, and $v_0(t) = v_{c1}(t) + v_{c2}(t)$. The governing equations for the circuit shown in Fig. 2(a) can be written as

$$v_g(t) = i_L R_g + L \frac{di_L}{dt} + \frac{1}{C_s} \int i_1 dt + V_1$$

$$v_0(t) = i_L R_L = \frac{1}{C_L} \int i_1 dt + V_1 + V_2. \hspace{1cm} (2)$$

During this mode, upper split capacitor ($v_{c1}(t)$) charges from the grid and lower split capacitor ($v_{c2}(t)$) discharges into load and grid. This mode ends when either diode $D_1$ stops conducting, current drawn from the grid goes to zero, or $v_{c2}(t)$ has fallen to zero.

B. Mode-II From $t_2 < t < t_3$

Mode-II starts at $t_2$ when diode $D_2$ starts conducting that is $v_{c2}(t_2) = 0$ and $D_1$ is already conducting. Let $v_{c1}(t_2) = V_{\text{mll}}$, and $i_L(t_2) = I_{L0}$. Fig. 2(b) shows the equivalent circuit and the equations for this mode can be written as

$$v_g(t) = i_L R_g + L \frac{di_L}{dt} + \frac{1}{C_s} \int i_1 dt + V_{\text{mll}}$$

$$v_0(t) = i_L R_L = \frac{1}{C_L} \int i_1 dt + V_{\text{mll}}. \hspace{1cm} (4)$$

As diode $D_2$ is conducting, this ensures that the lower split capacitor does not charge in opposite direction, so $v_{c2}(t)$ in this mode will remain zero. This mode ends when diode $D_1$ stops conducting.

### Table I

<table>
<thead>
<tr>
<th>Harmonic (n)</th>
<th>Limit (% of the Fundamental Input Current)</th>
</tr>
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<tbody>
<tr>
<td>3</td>
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</tr>
<tr>
<td>5</td>
<td>61</td>
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### Table II

<table>
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</tr>
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<tr>
<td>$V_o$</td>
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</tr>
<tr>
<td>$P_o$</td>
<td>25 W</td>
</tr>
<tr>
<td>$R_L$</td>
<td>5 Ω (1.08)</td>
</tr>
<tr>
<td>$L$</td>
<td>2 mH (136 μ)</td>
</tr>
<tr>
<td>$R_g$</td>
<td>5 Ω (1.08 m)</td>
</tr>
</tbody>
</table>

(a)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value (per unit)</th>
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<tbody>
<tr>
<td>$V_g$</td>
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</tr>
<tr>
<td>$P_o$</td>
<td>25 W (1)</td>
</tr>
<tr>
<td>$R_L$</td>
<td>5 Ω (1.08)</td>
</tr>
<tr>
<td>$L$</td>
<td>2 mH (136 μ)</td>
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<tr>
<td>$R_g$</td>
<td>5 Ω (1.08 m)</td>
</tr>
</tbody>
</table>

(b)

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**TABLE III**

Comparison of Standard Rectifier, Voltage Doubler, and SCFB Rectifier with Variation of $C_s$ and $C_L$

<table>
<thead>
<tr>
<th>$C_s$ ($\mu$F) (pu)</th>
<th>$C_L$ ($\mu$F) (pu)</th>
<th>$V_o$ (V) (pu)</th>
<th>$\Delta V$ (V) (pu)</th>
<th>THD (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>222 (322.6)</td>
<td>222 (322.6)</td>
<td>338 (1.0)</td>
<td>2.9 (8.5 m)</td>
<td>357</td>
</tr>
<tr>
<td>470 (666.7)</td>
<td>470 (666.7)</td>
<td>339 (1.0)</td>
<td>1.4 (4.1 m)</td>
<td>386</td>
</tr>
<tr>
<td>1000 (1.5 k)</td>
<td>1000 (1428.6)</td>
<td>340 (1.0)</td>
<td>0.8 (7.5 m)</td>
<td>394</td>
</tr>
<tr>
<td>2000 (3.3 k)</td>
<td>2000 (29.1)</td>
<td>340 (1.0)</td>
<td>0.3 (0.9 m)</td>
<td>395</td>
</tr>
<tr>
<td>2x10^6 (3.3 M)</td>
<td>222 (322.6)</td>
<td>338 (1.0)</td>
<td>2.9 (8.5 m)</td>
<td>357</td>
</tr>
</tbody>
</table>

Fig. 2. Different modes of operation for the SCFB rectifier. (a) Mode-I, (b) Mode-II, (c) Mode-III, and (d) Mode-IV.

conducting, that is the current drawn from the grid dies down to zero.

C. Mode-III From $t_3 < t < t_4$

Mode-III occurs when the current $i_L$ reaches zero at the end of Mode-I with $v_{C1}(t_2)$ and $v_{C2}(t_2) > 0$. In this case, time $t_3$ equals to the instant $t_2$, which is the end of Mode-I. In this mode, no diodes are conducting, therefore, the current from the grid is zero and load is supplied by the energy stored in capacitors $C_L$ and $C_s$. At $t = t_3$, let $v_{C1}(t_3) = V_{m_{III}}$ and $v_{C2}(t_3) = V_{m_{III}}$. Equivalent circuit for this mode is shown in Fig. 2(c), and the governing equations for this mode are

\[
v_0(t) = i_R R_L = v_{C1}(t) + v_{C2}(t)
\]

\[
v_0(t) = (V_{m_{III}} + V_{m_{III}}) e^{(t-t_3)/\tau_1}
\]

\[
\tau_1 = \frac{C_L + C_s}{2 R_L}
\]

D. Mode-IV From $t_4 < t < \frac{T}{2} + t_1$

Mode-IV occurs at the end of Mode-II when $i_L$ reaches 0 with $v_{C2}(t) = 0$. Hence, time $t_4$ matches with time $t_3$ of Mode-II. In this diode, $D_2$ is conducting and load is supplied by energy stored in capacitors $C_L$ and $C_s$. Let Mode-IV start at $t_4$ and $v_{C1} = V_{m_{IV}}$, the equivalent circuit is shown in Fig. 2(d) and the governing equations are given by

\[
v_0(t) = i_R R_L = v_{C1}(t)
\]

\[
v_0(t) = V_{m_{IV}} e^{(t-t_4)/\tau}
\]

\[
\tau = \frac{C_L + C_s}{R_L}
\]

The solutions of aforementioned differential equations for mode-I and mode-II are given in the Appendix. Analytical expressions in (6), (9), (11), (16), and (18) provide expressions for the capacitor voltage waveforms in terms of the circuit parameters. All remaining voltages and currents in the circuit can be obtained from these capacitor voltages.

For an input voltage of $V_g = 240$ V and load resistance of $R_L = 5$ k$\Omega$ (load power of around 22 W), the effect of variations in $C_L$ and $C_s$ on THD, $V_o$, and $\Delta V_o$ is shown in Fig. 3. From these results, it is seen that minimum THD is obtained when $C_s = 1.647$ $\mu$F for a particular value of $C_L$ and the value of $C_L$ is chosen such that $\Delta V_o$ is less than 1 V and it is 470 $\mu$F. It can also be observed, from Fig. 3(a) that the minimum of the THD is not significantly affected by $C_L$. It can also be seen from
Fig. 3. Circuit performance as a function of load capacitance and split capacitance showing (a) percentage THD, (b) output voltage ripple $\Delta V_o$, and (c) average output voltage $V_o$.

Fig. 3(b) that low values of $C_L$ leads to high ripple in the dc bus voltage. Also, Fig. 3(c) shows that larger values for $C_s$ lead to increase in the average dc bus voltage.

From Fig. 3(a), it can be concluded that by choosing a specific value of split capacitance ($C_s$), minimum THD injection can be obtained of a particular load. Also, Fig. 3(b) shows that output voltage ripple are mainly controlled by load capacitance ($C_L$), so THD and output voltage ripple can be controlled independently.

1) For a small value of the split capacitor ($C_s < 2 \mu F$), $v_{c2}(t)$ falls to zero before diode $D_1$ stops conducting in the positive half cycle of supply, then we get Mode-I followed by Mode-II. In this case, Mode I starts at $t_1 = 0$. For this mode, $v_g$, $i_L$, $v_{c1}$ and $v_{c2}$, and $V_o$ are shown in Fig. 4(a)–(c), respectively.

2) For a large value of the split capacitor ($C_s > 2 \mu F$), diode $D_1$ stops conducting before $v_{c2}(t)$ falls to zero in the positive half cycle of supply. In this case, Mode-I is followed by Mode-III. Also, in this case, the start of Mode-I is at $t_1 \neq 0$ and is delayed. For this case, $v_g$ and $i_L$, $v_{c1}$ and $v_{c2}$, and $V_o$ are shown in Fig. 4(d)–(f), respectively.

The dynamic equations for mode-I is solved assuming realistic initial conditions. The state of capacitor voltages and inductor current, at the end of mode-I, is the initial condition for mode-II. Using these initial conditions, dynamic equations for mode–II is solved. The states of dynamic variables at the end of a mode is the initial condition for the subsequent modes. Solutions, that is provided in the Appendix for the subsequent modes, are used to obtain the final circuit conditions at the end of the fundamental period. This procedure is continued till the steady-state solution for the dynamic variables is obtained. In steady state, the values of $C_s$ and $C_L$ is varied to get the optimal values of the ripple voltage in the output dc voltage and line-current THD. Fig. 3 shows the dependence of the output voltage, ripple in the output...
It is observed from analysis, simulation, and experiments that selection of capacitance parameters such that the initiation of Mode-III immediately after Mode-I leads to minimum source current THD. Fig. 5 shows the supply voltage and supply current for $L = 2 \text{ mH}$, $R_g = 5 \Omega$, $C_s = 1.65 \mu\text{F}$, $C_L = 470 \mu\text{F}$, and $R_L = 5000 \Omega$. For $R_L = 5000 \Omega$, $C_s = 1.65 \mu\text{F}$ corresponds to the lowest level of grid THD injection.

### IV. ANALYTICAL, SIMULATION, AND EXPERIMENTAL RESULTS

Analysis, simulation, and detailed experimental studies are performed for the proposed topology shown in Fig. 1(c). Design ratings of the converter are covered in Section II. Effects of line inductance, $L$, and load capacitance, $C_L$, in optimal split capacitance $C_s$, and THD in line current is also discussed in this section.

Fig. 5 shows the grid voltage and current drawn from the grid. Analytical results, shown in Fig. 5(a), simulation results, shown in Fig. 5(b), and experimental results, shown in Fig. 5(c), matches closely. THD of the current drawn from the grid for analytical, simulation, and experimental are 66.7%, 66.7%, and 62.5%, respectively. Table IV summarizes the harmonics, up to 500 Hz. This meets the IEC 61000-3-2 requirements specified in Table I. The small deviation in experimental measured THD is due to the nonzero resistances of the diode rectifier, which also shows in terms of the reduced oscillations in the waveform. Efficiency of the SCFB rectifier is measured to be 99.36% and that of the diode rectifier in Fig. 1(a) is 98.29% in experimental studies. This corresponds to a power loss reduction of 63% in the proposed SCFB topology. The higher efficiency of the SCFB rectifier is due to the reduction in conduction loss due to the lower RMS value of the input current when compared with the normal rectifier.

#### A. Effect of Line Inductance

Values of line inductance ($L$) varies from few micro-henry to few milli-henry. Effect of variations in $L$ on $C_s$ is shown in Fig. 6(a). It can be seen that values $C_s$ decreases with increase in $L$. For a particular value of $C_s = 1.65 \mu\text{F}$, effect of $L$ on line-current THD is shown in Fig. 6(b). In the circuit shown...
TABLE V
HARMONIC ANALYSIS OF THE EXPERIMENTALLY MEASURED LINE CURRENT DRAWN BY THE STANDARD RECTIFIER AND SCFB RECTIFIER WITH VARIATION IN $R_L$

<table>
<thead>
<tr>
<th>SCFB Rectifier</th>
<th>Percent Load (%)</th>
<th>$i_L$ RMS (A)</th>
<th>1st (% / A)</th>
<th>3rd</th>
<th>5th</th>
<th>7th</th>
<th>9th</th>
<th>11th</th>
<th>13th</th>
<th>15th</th>
<th>17th</th>
<th>19th</th>
<th>THD (%)</th>
<th>$V_{dc}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>0.264</td>
<td>100 / 0.2</td>
<td>20.3</td>
<td>39.6</td>
<td>22.3</td>
<td>30.5</td>
<td>31.0</td>
<td>15.2</td>
<td>22.8</td>
<td>17.8</td>
<td>20.3</td>
<td>89.21</td>
<td>339.0</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>0.19</td>
<td>100 / 0.16</td>
<td>45.0</td>
<td>20.6</td>
<td>18.8</td>
<td>16.9</td>
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<td>6.5</td>
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</tr>
<tr>
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<td>100 / 0.12</td>
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<td>20.8</td>
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<td>418.0</td>
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<td>100 / 0.104</td>
<td>71.2</td>
<td>31.7</td>
<td>9.6</td>
<td>17.3</td>
<td>10.6</td>
<td>3.8</td>
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<td>44.4</td>
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<td>18.9</td>
<td>11.1</td>
<td>11.1</td>
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<table>
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<th>3rd</th>
<th>5th</th>
<th>7th</th>
<th>9th</th>
<th>11th</th>
<th>13th</th>
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<td>99.6</td>
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<tr>
<td>25</td>
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<td>85.7</td>
<td>77.6</td>
<td>349</td>
<td>340.0</td>
<td></td>
</tr>
</tbody>
</table>

in Fig. 1(a), line-current THD decreases with increase in line inductance, but in the SCFB rectifier, the increase in $L$ and increase in the THD level by 10% as $L$ varies from 4 mH (272 μ, in per unit) to 10 mH (680 μ, in per unit).

B. Effect of Load Capacitance

The ripple in the output voltage decreases as the optimal load capacitance $C_L$ increases. Effect of variations in $C_L$ on $C_s$ is shown in Fig. 6(c). It can be seen that this value of $C_s$ remains a constant for $C_L$ greater than 10 μF. For a particular value of $C_{so} = 1.65$ μF, the effect of $C_L$ in line-current THD is shown in Fig. 6(d). As opposed the topology shown in Fig. 1(a), in an SCFB rectifier, the line-current THD remains almost a constant for higher values of load capacitance $C_L$. So, the value of $C_L$ can be chosen independently so that voltage ripple is within a desirable limit.

C. Effect of Load Variation

The value of split capacitance, $C_s$, is optimized for minimum THD in the line current for a particular load. Effect of load variation in line-current THD and output voltage is presented in this section. The value of $C_s$ is maintained at the same optimal value, optimized for rated load. Table V shows the summary of results of the SCFB rectifier and diode rectifier for different load conditions. In the diode rectifier, the output voltage, 340 V remains almost a constant for different load conditions.
In an SCFB rectifier, the line-current THD increases when the load varies. This happens because, the split capacitance value is optimized for rated load conditions. As the load on the converter decreases, the output voltage of the rectifier also increases. The effect of voltage doubling of the capacitor is causing this.

Fig. 7 shows the experimental results of the SCFB and diode rectifier for different load conditions. Fig. 7 shows the input voltage, blue waveform, line current, red waveform, and dc bus voltage, green waveform.

V. DESIGN INFERENCE BASED ON SCFB RESULTS

For the circuit shown in Fig. 1(c), if the input voltage is given by, \( v_g = A \sin \omega t \), then the current drawn from the grid can be expressed as

\[
i_L(\omega t) = \begin{cases} 
I_L \cos \omega t, & 0 \leq \omega t \leq \pi/2 \\
I_L \cos \omega t, & \pi \leq \omega t \leq 3\pi/2 \\
0, & \text{otherwise.}
\end{cases}
\]  

The underlying cosinusoidal nature and corresponding conduction durations of \( i_L(t) \) can be observed from the waveforms in Fig. 5. The current drawn from the grid is also given by

\[
i_L(t) = 2C_s \frac{dv_g}{dt}
\]  

\[
i_L(t) = 2C_s A\omega \cos \omega t.
\]
This is assuming that the load capacitance $C_L$ is large enough, such that the ripple in the output voltage is neglected. So, the magnitude of the output voltage is the peak of grid voltage, $A$. The load current is given by

$$i_R = \frac{A}{R_L}. \quad (15)$$

The power drawn by the load is given by

$$P_s = \frac{A^2}{R_L}. \quad (16)$$

Fig. 8 shows how energy is transferred in the SCFB rectifier. If the passive elements involved in the energy transfer are assumed to be ideal, the load power equals the power drawn from the grid, $P_{in}$. The input power is calculated as

$$P_{in} = \frac{A^2}{\pi} \int_0^{\pi/2} 2C_s A^2 \omega \sin(\omega t) \cos(\omega t) \, dt \quad (17)$$

$$P_{in} = \frac{A^2 \omega C_s}{\pi}. \quad (18)$$

Since all the elements involved are ideal, $P_{in} = P_o$, hence

$$\frac{A^2 \omega C_s}{\pi} = \frac{A^2}{R_L} \quad (19)$$

$$\therefore \quad C_s = \frac{\pi}{\omega R_L}. \quad (20)$$

Based on (20) $C_s$ is evaluated to be 2 $\mu$F. This is approximately equal to 125% of the optimal value. Fig. 9 shows the simulation results for the circuit shown in Fig. 1(a) and matches with (12). In the presence of line inductance, the initial step in $i_L(t)$ is replaced by oscillations in the current due to the circuit elements $L$ and $2C_s$. Fig. 5(b) shows the simulations results when the line inductance is 2 mH and line resistance is 5 $\Omega$. The natural frequency of oscillation is verified be 11.18 k rad/s with damping ratio of 0.1118.

Using the initial estimate for $C_s$ from (20), one can then use the exact circuit solution to obtain the optimal $C_s$ as described in Section III.

VI. CONCLUSION

In this paper, an SCFB rectifier is proposed to reduce the harmonic injection in the line by using capacitive components. Two capacitances (X rated) are used to affect the input line current so that input line-current harmonics are reduced. The analytical modeling of the new topology is systematically performed. The results are verified with simulation results and experimental results. The analytical model is used to find the value of capacitances $(C_s)$ for which minimal line-current THD can be obtained for a particular load. Also it is shown that ripple in the output voltage can be independently controlled by load capacitance $(C_L)$. The proposed rectifier circuit also operates with a higher efficiency compared to standard rectifiers.

APPENDIX

The output voltage and input line current provide information about the performance characteristics of a rectifier. Equations, which are obtained by analysis in Mode-I and Mode-II of the SCFB rectifier, are solved below to obtain analytical expressions for $\psi(t)$ and $i_L(t)$.

A. SCFB Rectifier

1) Mode-I From $t_1 < t < t_2$: Equations (1) and (2) in Section III-A form a fourth-order system. The roots of the characteristic equation are solved assuming well-separated circuit poles [5].

$$
\psi(t') = -V_m \frac{\omega^2}{\omega_d} y \left[ A_4 e^{-\psi t'} + B_4 \cos(\omega t') + C_4 \sin(\omega t') + e^{-\xi \omega t'} \frac{-D_4}{\sqrt{1 - \xi^2}} \sin(\omega_d t' + \phi) + C_4 \frac{\omega_d}{\omega_d^2} \sin(\omega_d t') \right]
$$

where

$$\omega_d = \sqrt{\frac{R_L(C_s + C_L) + 2C_s R_g}{R_L LC_s (C_s + 2C_L)}} \quad (22)$$

$$\chi = \frac{1}{R_L(C_s + C_L) + 2C_s R_g} \quad (23)$$

$$\xi = \frac{2L C_s + R C_s R_g (C_s + 2C_L)}{2 \sqrt{L C_s R_L (C_s + C_L)}[\chi R_L (C_s + 2C_L) + 2C_s R_g]} \quad (24)$$

$$\psi(t') = \frac{\omega_n}{\sqrt{1 - \xi^2}} y \left[ A_5 e^{-\psi t'} + e^{-\xi \omega t'} \right] \sin(\omega_d t' + \phi) + C_5 \frac{\omega_d}{\omega_d^2} \sin(\omega_d t') \quad (21)$$

$$\omega_n = \sqrt{\frac{R_L(C_s + C_L) + 2C_s R_g}{R_L LC_s (C_s + 2C_L)}} \quad (22)$$

$$y = \frac{1}{R_L(C_s + C_L) + 2C_s R_g} \quad (23)$$

$$\xi = \frac{2L C_s + R C_s R_g (C_s + 2C_L)}{2 \sqrt{L C_s R_L (C_s + C_L)}[\chi R_L (C_s + 2C_L) + 2C_s R_g]} \quad (24)$$

$$\omega_d = \sqrt{1 - \xi^2}, \quad \phi = \tan^{-1} \sqrt{1 - \xi^2} \xi \quad (25)$$
where $
abla$ is given by

\[
\nabla = \begin{bmatrix}
1 & 1 & 0 \\
2\xi\omega_n & y & 1 \\
\omega_n^2 & \omega_n^2 & \omega_n^2
\end{bmatrix}
\]

\[
i_L(t') R_y + L \frac{di_L(t')}{dt'} = v_y(t') - v_y(t'') + v_C2(t').
\]  

(27)

The solutions for $v_y(t)$ in (11) and $v_{C2}(t)$ in (16) is used to evaluate $i_L(t)$ in (17).

2) Mode-II From $t_2 < t < t_3$

\[
v_y(t'') = \frac{V_m (R_L + R_y)}{R_L L (C_L + C_s)} \left[ A_0 \cos \omega t'' + \frac{B_0}{\omega} \sin \omega t'' + C_0 e^{-\nu t''}
\right.

\]

\[
+ D_0 e^{-\eta t''} + \frac{i_L(t_2) (R_L + R_y)}{R_L (q - p) (C_L + C_s)} \left[ e^{-\nu t''} - e^{-\eta t''}
\right]
\]

\[
+ \frac{2R_L}{L} \frac{2R_L}{L} - (p + q)
\]

\[
\times \left( e^{-\nu t''} - e^{-\eta t''}\right)
\]

(28)

where

\[
p = \frac{L + R_L R_y (C_L + C_s)}{2LRL (C_L + C_s)}
\]

\[
+ \sqrt{\left( \frac{L + R_L R_y (C_L + C_s)}{2LRL (C_L + C_s)} \right)^2 - \frac{R_L + R_y}{LR_L (C_L + C_s)}}
\]

\[
q = \frac{L + R_L R_y (C_L + C_s)}{2LRL (C_L + C_s)}
\]

\[
- \sqrt{\left( \frac{L + R_L R_y (C_L + C_s)}{2LRL (C_L + C_s)} \right)^2 - \frac{R_L + R_y}{LR_L (C_L + C_s)}}
\]

\[
A_6 = \nabla^{-1} \times \begin{bmatrix}
0 & 0 & 0 & 0 \\
\sin \omega t_2 & \omega \cos \omega t_2
\end{bmatrix}
\]

(29)

Knowing the grid voltage and $V_o(t)$ in (18), the input current $i_L(t)$ is solved in Mode-II. The expressions for the source current and output voltage are used to obtain THD and voltage design tradeoff relationship shown in Fig. 3.
REFERENCES


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