Design and Control of High Frequency, High Power Amplifier for Network Analyzers

A Project Report
Submitted in Partial Fulfilment of Requirement for the Degree of Master of Engineering in Electrical Engineering

By
Prashanth Manikumar Chennamsetty

Department of Electrical Engineering
Indian Institute of Science
Bangalore - 560 012
India

June 2012
Acknowledgements

I express my profound gratitude deep from the apex of my heart to Dr. Vinod John for providing me with an opportunity to work in the field of Power Electronics and suggesting me a challenging project. I sincerely thank him for his generous support, guidance and constructive engagement throughout my project work. His thought provoking ideas and simplistic approaches to complex problems influenced my work in a great way.

His excellent courses on Dynamics of Linear Systems and Topic in Power Electronics and Distributed Generation were very helpful for my project work.

I am grateful to Dr. G. Narayanan for his wonderful lectures on Pulse Width Modulated Converters and Applications. His ideas of viewing problems from different perspectives to get simple solution, his humble nature and simplicity have been a true inspiration. I am thankful to Dr. V. Ramanarayanan and (late) Dr. V. T. Ranganathan for their marvelous course notes on Switched Mode Power Converters and Electric Drives respectively.

I would also like to thank Dr. P. S. Nagendra Rao and Dr. M. K. Gunasekaran for their excellent courses on Advanced Computer Aided Power System Analysis and Electromagnetic compatibility respectively.

I am grateful to all the professors of Indian Institute of Science who have imparted knowledge to me. I thank the Government of India for the financial support provided to me.

I thank Mr. Ravi and Mr. Ramachandran for their help in designing bus-bars for power circuit and for teaching me how to work with various workshop tools.

I sincerely thank Mrs. Silvi Jose for her help in purchase of components etc. I would also like to thank Mr. D. M. Channe Gowda and his colleagues at the EE Office who have always been very helpful.

I am also grateful to Ms. Suma of Newtech technologies who helped me a lot in the layout of the PCBs.
I thank my B. Tech lecturer Mrs. Madhuri for introducing Power Electronics to me. I also like to thank my childhood teachers Mr. Kalyan Ram and Mrs. Sri Devi who helped me to figure out my inner capabilities and helped to fulfil my dreams. They will be remembered for ever.

I would like to thank Shiva Prasad, Anirban, Soumitro, AKP, Pavan Hari, Asish and Anirudh for their academic discussions related to my project. I thank my ME seniors Abhijit, Sujata and Debasish for their support and encouragement throughout my project work. I especially like to thank Sethupathy for practically showing me that *Time is Non-renewable resource*. His humorous talks made me forget all my worries during my project work.

My stay at IISc has been memorable because of my loving friends. I thank Akshay, Amit, Arun, Krishna, Manu, RP, Vikash and Sudarshan for their fruitful technical and non-technical discussions. I would also like to thank all my other friends for their extensive support.

My life would be meaningless if I do not mention my parents. Believe it or not – There is not even a single day they did not call me in these two years for knowing about my wellness. I bow to them and thank them for their encouragement, support and faith in me. Without their love and help whatever I have achieved would be impossible.

Last but not the least, I thank God Almighty for giving me will power and for making the things go smoothly.
Abstract

In the Field of Power Electronics and Electric Drives, characterization of different electrical machines and power components like induction machines, transformers, capacitors etc. play a significant role. The behavior of high power devices is different at different frequencies. High frequency models and low frequency models of different machines are critical to design a controller for the solid state converters driving them. Network Analyzers or Frequency Response Analyzers (FRAs) are the equipment used for characterizing electrical machines and power components over wide range of frequencies ranging from few millihertz to tens of Megahertz.

Network Analyzers have a source port which generates a sinusoidal signal of less than 10 Volts peak-peak with a wide range of sweep frequencies and two measurement ports for estimating the amplitude and phase between the output signals from Device Under Test (DUT). Source port of network analyzer can supply a maximum current of 0.707 Amperes peak-peak. When characterization of high power components and machines is done with such weak excitation signals, errors due to noise signals are predominant. Hence there are standards for characterizing high power devices.

To characterize high power devices, we need power levels greater than the standard network analyzers output power capability and sweep frequencies from tens of millihertz to hundreds of Hertz. Hence, we need a power amplifier between the network analyzer and the Device Under Test (DUT). Also, we need to limit output current of the power amplifier, so as not to damage DUT and the power amplifier itself. According to IEEE Std 115A-1987, test currents should not exceed one-half of one percent of rated device current.

The present project aims at designing a power amplifier (class-D) with maximum output voltage of 20 Volts peak-peak, maximum output current of 20 Amperes peak-peak and
operating frequencies varying from 10 Hz to 5 kHz. The designed power amplifier has the
capability to dynamically change control modes between voltage mode control and current
mode control depending on the output voltage and current of amplifier. Hence, using this
amplifier we can also characterize a machine having an output current capability of 1400
Amperes.

Since the operating frequencies of Class-D amplifier is up to 5 kHz, the switches used
should switch at very high frequencies. This demands the high speed processors and switching devices, making the amplifier costly. Also, designing the controller at different operating
frequencies of the amplifier, to limit output current and voltage is critical. All the difficulties
are addressed with low speed processors and switching devices and the cost effective solutions
are suggested.
## Contents

<table>
<thead>
<tr>
<th>Acknowledgements</th>
<th>i</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abstract</td>
<td>iii</td>
</tr>
<tr>
<td>List of Tables</td>
<td>viii</td>
</tr>
<tr>
<td>List of Figures</td>
<td>ix</td>
</tr>
</tbody>
</table>

### 1 Introduction

1.1 Overview of the project .................................. 2
1.2 Organization of the report ................................ 3
1.3 Conclusion .................................................. 4

### 2 Topology of the Amplifier and its Design

2.1 Introduction .................................................. 5
2.2 6 - Leg Full bridge Single phase inverter ............... 6
    2.2.1 Operation of the 6 - Leg Inverter .................... 6
    2.2.2 7 - Level PWM Output Voltage ....................... 8
2.3 Switching device selection and Loss calculation ....... 11
    2.3.1 Conduction Loss .................................. 12
    2.3.2 Switching loss .................................... 13
    2.3.3 Total loss ......................................... 13
2.4 Heat sink thermal analysis .................................. 14
2.5 Design of dc bus capacitance ............................... 19
    2.5.1 Calculation of double frequency component ripple .. 19
    2.5.2 Calculation of switching frequency ripple .......... 20
Chapter 2: Phase Shifted Carrier (PSC) generation

2.6 Phase Shifted Carrier (PSC) generation

2.6.1 Analog circuit for PSC generation and its stability analysis

2.6.2 Sequential circuit implementation in FPGA

2.6.3 Features of PSC generation board

2.6.4 Testing of PSC generation board

Chapter 2: Auxiliary circuits of Inverter

2.7 Auxiliary circuits of Inverter

2.7.1 Protection and Delay card

2.7.2 Gate drive cards

2.7.3 Current sensing cards

Chapter 2: Conclusion

Chapter 3: Output Filter Design and Circulating Current Mitigation

3.1 Introduction

3.2 Design of L filter

3.2.1 Calculation of filter inductance

3.2.2 Design procedure

3.3 Circulating currents in Parallel inverters

3.3.1 Concept of Differential Mode Inductor

3.3.2 DMI design for 3-Leg half bridge inverter

Chapter 3: Conclusion

Chapter 4: Closed Loop Control Design

4.1 Introduction

4.2 Digital controller

4.2.1 FPGA board

4.2.2 ADC

4.2.3 DAC

4.3 Block diagram of the controller

4.4 Digital implementation of control blocks

4.4.1 Peak detector

4.4.2 Current / Voltage mode decisive circuit

4.4.3 Per-unit Values

4.5 Conclusion
5 Simulation and Experimental Results 51
  5.1 Introduction .................................................. 51
  5.2 Simulation results ............................................. 51
  5.3 Experimental results ......................................... 53
  5.4 Conclusion .................................................... 61

6 Conclusions 63
  6.1 Summary of the present work ............................... 63
  6.2 Suggestions for future work ................................. 64

A Phase Shifted Carrier Generation Board Schematics and its operation de-
tails 65
  A.1 Operation details of PSC generation board ................. 83

B Interleaved Interface Board Schematics 85

C Pictures of Hardware 89

References 93
## List of Tables

1.1 Specifications of Network Analyzer .............................................. 1
2.1 Possible combinations of operating regions .................................. 10
2.2 Possible voltage levels in output PWM waveform ............................. 10
2.3 Specifications of Inverter .......................................................... 11
2.4 Unit losses with Interleaved carriers ......................................... 14
2.5 Unit losses without Interleaved carriers ($f_m = 5.2 \text{ kHz}$) .......... 14
2.6 Specifications of Heat sink ......................................................... 15
2.7 High frequency DC Bus capacitor ripple current comparison .......... 23
2.8 State table for generation of 120° phase shifted square waves .......... 28
3.1 Specifications of Output Filter Inductor ...................................... 35
3.2 Specifications of Differential Mode Inductor .................................. 39
4.1 Specifications of ALTERA FPGA device ................................. 43
4.2 Truth table of Current / Voltage mode decisive circuit .................. 48
4.3 Per Unit values ............................................................................. 49
5.1 Simulation parameters .................................................................. 51
A.1 Bill of Materials for one channel PSC generation board ................. 82
List of Figures

1.1 Block diagram of the project .......................... 2

2.1 6 - Leg Full bridge Single phase inverter ....................... 6

2.2 (a) Modulation signals comparison against phase shifted carriers (b) PWM voltage of 1st H-bridge (c) PWM voltage of 2nd H-bridge (d) PWM voltage of 3rd H-bridge (e) Output PWM voltage of inverter ................... 7

2.3 Operating regions of a Unit .................................... 8

2.4 States and Equivalent circuits of Unit in operating region 1 .......................... 9

2.5 States and Equivalent circuits of Unit in operating region 2 .......................... 9

2.6 States and Equivalent circuits of Unit in operating region 3 .......................... 9

2.7 Total possible states of a Unit ................................... 9

2.8 Simulated No - Load voltage of Inverter (simulation done in MATLAB 7.0) .................. 11

2.9 Experimental No - Load voltage of Inverter (Pink) and Modulating signal (Blue) .......................... 11

2.10 Parallel plate-fin heat sink .......................... 15

2.11 Thermal model of Unit of the Inverter .......................... 17

2.12 Heat sink thermal resistance Versus Ambient temperature .......................... 18

2.13 Maximum allowable power loss per switch Versus Ambient temperature .......................... 18

2.14 (a) Bands showing 2 different operating states of Unit I (b) Capacitor current due to switching of Unit I (c) ON state switches of Unit I in blue shaded band (d) ON state switches of Unit I in pink shaded band .......................... 21

2.15 (a) Carrier signals and modulation signals of Inverter (b) Capacitor current due to switching of Unit I (c) Capacitor current due to switching of Unit II (d) Total DC bus capacitor current .......................... 22

2.16 Block diagram of Phase Shifted Carrier generation circuit .......................... 24

ix
List of Figures

2.17 Circuit diagram of Phase Shifted Carrier generator ........................................... 25
2.18 Detailed block diagram of Phase Shifted Carrier generation circuit ...................... 26
2.19 Bode plot of open loop transfer function of PSC generation circuit ..................... 26
2.20 State diagram for 3-phase square wave generation ............................................ 27
2.21 Carrier signal of frequency 416 kHz from PSC generation board - 5 V/div ........... 29
2.22 Sine-triangle PWM — CH1(Green, 1 V/div): Sinusoidal modulation signal of frequency 50 Hz; CH2(Blue, 1 V/div): Triangular carrier signal of frequency 1.6 kHz; CH3(Pink, 20 V/div): PWM Pulses of 1.6 kHz ........................................ 29
2.23 $120^\circ$ phase shifted square waves of 52 kHz frequency from FPGA controller ....... 30
2.24 $120^\circ$ phase shifted carrier signals of 52 kHz frequency from PSC generation board .......................................................... 30
3.1 Average model of one H-bridge in 6-Leg inverter ............................................. 34
3.2 (a) Structure of Differential mode inductor (b) Circuit Symbol ............................... 36
3.3 Structure of DMI for 1-$\phi$ parallel half bridge inverters ...................................... 37
4.1 Block diagram of FPGA based digital platform ............................................... 42
4.2 Block diagram of closed loop controller ............................................................ 44
4.3 Timing diagram and related waveforms of the Peak detector ............................... 45
4.4 Digital circuit to obtain $x[n]$ waveform ............................................................ 46
4.5 (a) Digital circuit to obtain $y[n]<0$ (b) Digital circuit to obtain $y[n]>0$ ............. 47
4.6 (a) Digital circuit to obtain a pulse at positive zero crossing (b) Digital circuit to obtain a pulse at negative zero crossing .......................................................... 47
4.7 Sampling circuit to obtain Peak value of $y[n]$ ..................................................... 47
4.8 Current / Voltage mode decisive circuit ............................................................ 48
5.1 Simulated output current of 6-Leg inverter at an operating frequency of 5.2 kHz .... 52
5.2 Simulated Leg current of 6-Leg inverter at an operating frequency of 5.2 kHz ....... 52
5.3 Simulated circulating current of 6-Leg inverter at an operating frequency of 5.2 kHz .......................................................... 53
5.4 Modulation signal from controller during soft start - 2.5 V/div, 1 s/div ............... 54
5.5 CH1(Blue, 50 V/div): Output voltage; CH2(Orange, 1 A/div): Load current; CH3(Green, 2 A/div): Leg A current; CH4(Pink, 2 A/div): Leg B current; MATH CH(Cyan, 1 A/div): Circulating current — $f_m=5.2$ kHz ................................. 54
List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.6</td>
<td>CH1(Blue, 1 A/div): Load current; CH2(Pink, 10 V/div): Output voltage —</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td>$f_m = 4.4$ kHz</td>
<td></td>
</tr>
<tr>
<td>5.7</td>
<td>CH1(Blue, 1 A/div): Load current; CH2(Pink, 10 V/div): Output voltage —</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td>$f_m = 3.0$ kHz</td>
<td></td>
</tr>
<tr>
<td>5.8</td>
<td>CH1(Blue, 2 A/div): Load current; CH2(Pink, 10 V/div): Output voltage —</td>
<td>56</td>
</tr>
<tr>
<td></td>
<td>$f_m = 2.0$ kHz</td>
<td></td>
</tr>
<tr>
<td>5.9</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage —</td>
<td>56</td>
</tr>
<tr>
<td></td>
<td>$f_m = 1.0$ kHz</td>
<td></td>
</tr>
<tr>
<td>5.10</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage —</td>
<td>57</td>
</tr>
<tr>
<td></td>
<td>$f_m = 880$ Hz</td>
<td></td>
</tr>
<tr>
<td>5.11</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage —</td>
<td>57</td>
</tr>
<tr>
<td></td>
<td>$f_m = 725$ Hz</td>
<td></td>
</tr>
<tr>
<td>5.12</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage —</td>
<td>58</td>
</tr>
<tr>
<td></td>
<td>$f_m = 625$ Hz</td>
<td></td>
</tr>
<tr>
<td>5.13</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage —</td>
<td>58</td>
</tr>
<tr>
<td></td>
<td>$f_m = 500$ Hz</td>
<td></td>
</tr>
<tr>
<td>5.14</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Pink, 5 V/div): Output voltage —</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td>$f_m = 200$ Hz</td>
<td></td>
</tr>
<tr>
<td>5.15</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Pink, 2.5 V/div): Output voltage —</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td>$f_m = 100$ Hz</td>
<td></td>
</tr>
<tr>
<td>5.16</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Pink, 2.5 V/div): Output voltage —</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>$f_m = 60$ Hz</td>
<td></td>
</tr>
<tr>
<td>5.17</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Green, 2 A/div): Leg current; —</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>CH3(Pink, 2.5 V/div): Output voltage — $f_m = 50$ Hz [CRO in average mode]</td>
<td></td>
</tr>
<tr>
<td>5.18</td>
<td>CH1(Blue, 5 A/div): Load current; CH2(Green, 2 A/div): Leg current; —</td>
<td>61</td>
</tr>
<tr>
<td></td>
<td>CH3(Pink, 2.5 V/div): Output voltage — $f_m = 29.3$ Hz [CRO in average mode]</td>
<td></td>
</tr>
<tr>
<td>A.1</td>
<td>Phase shifted carrier generator - Channel 1</td>
<td>67</td>
</tr>
<tr>
<td>A.2</td>
<td>PWM pulse generator - Channel 1</td>
<td>68</td>
</tr>
<tr>
<td>A.3</td>
<td>Phase shifted carrier generator - Channel 2</td>
<td>69</td>
</tr>
<tr>
<td>A.4</td>
<td>PWM pulse generator - Channel 2</td>
<td>70</td>
</tr>
<tr>
<td>A.5</td>
<td>Phase shifted carrier generator - Channel 3</td>
<td>71</td>
</tr>
<tr>
<td>A.6</td>
<td>PWM pulse generator - Channel 3</td>
<td>72</td>
</tr>
</tbody>
</table>
A.7 Phase shifted carrier generator - Channel 4 .................................................. 73
A.8 PWM pulse generator - Channel 4 ................................................................. 74
A.9 Phase shifted carrier generator - Channel 5 .................................................... 75
A.10 PWM pulse generator - Channel 5 ................................................................. 76
A.11 Phase shifted carrier generator - Channel 6 ................................................... 77
A.12 PWM pulse generator - Channel 6 ................................................................. 78
A.13 Solder side layout of PSC generation board .................................................. 79
A.14 Component side layout of PSC generation board ......................................... 80
A.15 Top legend of PSC generation board ............................................................. 81

B.1 Interleaved Interface Board ............................................................................. 87
B.2 Solder side layout of Interface Board .............................................................. 88
B.3 Top legend of Interface Board ......................................................................... 88

C.1 (1) Phase Shifted Carrier generation board (2) Interface board ....................... 91
C.2 Experimental setup - (1) Unit I of Inverter (2) Unit II of Inverter (3) PSC generation board (4) FPGA digital controller (5) Load Inductor (6) Differential Mode Inductor (7) Filter Inductor ................................................................. 91
Chapter 1

Introduction

Network Analyzers are the equipment used to obtain frequency responses and for characterizing power components such as inductors, capacitors, machines and switched mode power supplies [8]. Characterization is done from few millihertz to tens of Megahertz using a sweep sine signal. Sweep signal of any standard network analyzer is very weak that external noise signals may result in erroneous characterization of Device Under Test (DUT). When characterizing any high power devices, the following conditions are to be met —

- Excitation current should be high enough to see the effect of parasitics at high and low frequencies [6] and should not exceed one half of 1% of device rated current [17].

- Sweep frequencies should be from 1 mHz to 200 Hz [15][16].

Hence, a power amplifier is required in between the network analyzer and the DUT to boost the power level of the sweep signal and its operating frequency has to be from few millihertz to hundreds of Hertz. The network analyzer considered for the present project is AP Instruments Model 200 and its specifications are given in table 1.1.

<table>
<thead>
<tr>
<th>SI.No.</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Maximum Sweep signal voltage</td>
<td>2.5 V pk-pk</td>
</tr>
<tr>
<td>2</td>
<td>Maximum Sweep signal current</td>
<td>0.707 A pk-pk</td>
</tr>
<tr>
<td>3</td>
<td>Sweep frequency range</td>
<td>0.01 Hz (&lt; f_{\text{sweep}} ) &lt; 15 MHz</td>
</tr>
<tr>
<td>4</td>
<td>Output Impedance</td>
<td>100 Ω</td>
</tr>
</tbody>
</table>

This chapter gives the broad overview of the project using the block diagram and also the organization of the report.
1.1 Overview of the project

A brief explanation of stages of work involved in the project is explained in this section using the block diagram shown in Fig. 1.1.

![Figure 1.1: Block diagram of the project](image)

Power Amplifier

Class D Amplifiers using Pulse Width Modulated techniques are the good solutions to have higher output currents. The power amplifier should be able to replicate a modulating signal of at least 100 kHz to get good frequency response of a high power DUT. A single phase inverter is used as a Class D amplifier in this project. Hence, the carrier frequency should be at least 1 MHz to replicate the modulating wave of 100 kHz. But to generate PWM signals for the inverter at 1 MHz, we need high speed digital processors. This will make the system costly. So, a multi leg single phase inverter topology is used in which each switch of inverter switches at low frequency but the output PWM voltage will be of high frequency.
1.2 Organization of the report

PWM Generator

The PWM generator consists of a triangular carrier wave generation circuit and a comparator circuit to compare the modulating wave against the carrier wave to generate PWM gate pulses. Carrier wave frequency is decided by the switching frequency of an Inverter. Since the clock frequency of any digital controller is bottle neck to generate high frequency triangular waveforms of sufficient magnitude with good resolution, an analog circuit has to be designed to get the job done.

Digital Controller

A digital controller is mainly used to control the output current of the inverter by continuously monitoring its output current and voltage and varying the amplitude of modulating signal. A closed loop controller has been designed by using an FPGA control board in this project.

Attenuator

The input and output signals of the high power DUT will have higher power than the measurement capability of network analyzer. Hence, before feeding these signals to measurement ports of network analyzer we should attenuate them using an attenuator. The attenuator designed should not cause any significant delay in measurement and it should not interfere with the measurements being made.

Isolation

Isolation between low power network analyzer and high power amplifier is needed to avoid damage to the network analyzer under the event of faults on power amplifier. Isolation makes it possible to test high power DUT that may be grounded or floating up to a voltage level of 600 V.

1.2 Organization of the report

Chapter 2 discusses about the overall design of Inverter. It explains the topology of the inverter, its operation and design of DC bus capacitors, heat sink and PWM generation
circuit. It also addresses the usage of different auxiliary circuits to achieve different objectives involved.

Chapter 3 is dedicated to issues of circulating currents in Multi leg inverters, their mitigation by passive filtering and design of output filter inductor to filter the current ripple.

Chapter 4 explains the details of closed loop controller design and how different elements are implemented in FPGA digital controller.

Chapter 5 presents the simulation results and experimental results to validate different ideas implemented.

1.3 Conclusion

This chapter addressed the issues in characterizing high power devices and gave a complete overview of the project. In the end, it discussed how the report is organized in a nutshell.
Chapter 2

Topology of the Amplifier and its Design

2.1 Introduction

Characterization of high power devices demands excitation currents beyond the output current capability of Network Analyzers. Class – D Amplifiers have the capability to give high output current. Conventional Class – D Amplifiers are Half bridge inverter and Full bridge inverter. Output voltage signal of frequencies beyond few tens of kilohertz from the Class D Amplifier requires the switches to be switched at 100 kHz and higher. This calls for high speed processors and switching devices which makes the system costly.

To avoid the use of high speed devices, a 6 – Leg single phase inverter with Phase Shifted Carrier Modulation is used. Use of Multi leg inverters have following advantages:

- Current rating of the switches reduces
- Output voltage will have more number of levels which reduces its distortion
- Output PWM switching frequency will be more than the switching frequency of the switching devices
- Reduction of DC Bus capacitor ripple current

The only disadvantage of Multi leg inverters is complexity in control of circulating currents between different legs.
2.2 6 - Leg Full bridge Single phase inverter

The topology of the Inverter used in the project is shown in Fig. 2.1. This is a single phase full bridge inverter with 6 legs. It is evident that this topology is obtained by connecting 3 H — bridge inverters in parallel on both AC side and DC side. This section explains its operation in detail and presents the simulated output PWM voltage to validate the theory.

![Diagram](image)

Figure 2.1: 6 - Leg Full bridge Single phase inverter

2.2.1 Operation of the 6 - Leg Inverter

Parallel inverters are generally used to increase the power rating of the system. But for the present application, we take the advantage of increased output PWM switching frequency by the method of carrier interleaving. Since the topology has 3 H – bridges connected in parallel on both AC side and DC side, they are operated using three different triangular carriers for sine – triangle PWM. The three carrier signals for the inverter are phase shifted by 120° so as to have minimum distortion in the output voltage.

The output voltage of the inverter is average of the output voltages of 3 H – Bridges. In an H – bridge inverter, for each carrier cycle we have 2 PWM pulses. When we phase shift the carriers by 120°, the pulses are also phase shifted by 120°. Hence, when the phase shifted pulses are added, we have 6 pulses for every carrier cycle. This is clearly shown in Fig. 2.2

The topology used will increase the output PWM switching frequency by 3 times when compared with the H – bridge inverter topology. This fact will allow us to use the existing auxiliary circuits and switching devices of low operating frequency. Also, we will have 7 levels in the output PWM voltage and hence making the filter size reduced.
Figure 2.2: (a) Modulation signals comparison against phase shifted carriers (b) PWM voltage of 1\textsuperscript{st} H-bridge (c) PWM voltage of 2\textsuperscript{nd} H-bridge (d) PWM voltage of 3\textsuperscript{rd} H-bridge (e) Output PWM voltage of inverter
2.2.2 7-Level PWM Output Voltage

Consider the left group of 3 legs in the inverter shown in Fig. 2.1 as Unit I and right group as Unit II. The modulating signal for all the legs in corresponding unit is same. Further, as in case of Sine – Triangle PWM of H – bridge, the modulating signal of Unit II is the inverted modulating signal of Unit I. The two switches in any leg operate in complimentary fashion to avoid DC bus short circuit.

To get clarity about the number of levels in PWM output voltage, let us divide the phase shifted carriers into 3 regions as shown in Fig. 2.3. The modulating signal of a unit can be only in any one of the regions shown in Fig. 2.3. Let us consider the state of a leg as 1 if its top switch is ON and 0 if its bottom switch is ON.

Fig. 2.4 shows the states of the legs and equivalent circuits of the unit when its modulating signal is in region 1. The states of the legs are indicated with the colour corresponding to its carrier signal in Fig. 2.4(a). The Unit operating in this region have four different states – 011, 101, 110 and 111. The equivalent circuit shown in Fig. 2.4(b) correspond to the states 011, 101 and 110 and the one shown in Fig. 2.4(c) correspond to state 111. Hence the output voltage of the Unit can be either \( \frac{2}{3} V_{DC} \) volts or \( V_{DC} \) volts with respect to negative DC bus.

Similar explanation can be given for the Unit operating in regions 2 and 3. The states of the legs and equivalent circuits of the unit when the modulating signal is in region 2 and region 3 is shown in Fig. 2.5 and Fig. 2.6 respectively. When operating in region 2, output voltage of the Unit can be either \( \frac{2}{3} V_{DC} \) volts or \( \frac{V_{DC}}{3} \) volts with respect to negative DC bus and when operating in region 3, it can be either \( \frac{V_{DC}}{3} \) volts or 0 volts with respect to negative DC bus. Total possible states of a Unit is shown in Fig. 2.7.
2.2. 6 - Leg Full bridge Single phase inverter

Figure 2.4: States and Equivalent circuits of Unit in operating region 1

Figure 2.5: States and Equivalent circuits of Unit in operating region 2

Figure 2.6: States and Equivalent circuits of Unit in operating region 3

Figure 2.7: Total possible states of a Unit
When Unit I is operating in region 1, Unit II will operate in region 3 and vice versa. But when Unit I is operating in region 2, Unit II will also operate in region 2. Table 2.1 shows the possible combinations of operating regions for Unit I and Unit II together.

### Table 2.1: Possible combinations of operating regions

<table>
<thead>
<tr>
<th>Combination No.</th>
<th>Unit I Operating region</th>
<th>Unit II Operating region</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Region 1</td>
<td>Region 3</td>
</tr>
<tr>
<td>2</td>
<td>Region 2</td>
<td>Region 2</td>
</tr>
<tr>
<td>3</td>
<td>Region 3</td>
<td>Region 1</td>
</tr>
</tbody>
</table>

Since in each region of operation we have 2 possible output voltages for a Unit, there will be 4 different combinations of output voltages for each combination of operating regions of Units. All the levels in output PWM voltage for every combination is given in Table 2.2. Hence we can see that, neglecting the repetitions we have 7 levels in output PWM voltage — $0$, $-V_{DC}/3$, $V_{DC}/3$, $-2V_{DC}/3$, $2V_{DC}/3$, $-V_{DC}$ and $V_{DC}$.

### Table 2.2: Possible voltage levels in output PWM waveform

<table>
<thead>
<tr>
<th>SI. No.</th>
<th>Output voltage of Unit I w.r.t $-ve$ DC bus</th>
<th>Output voltage of Unit II w.r.t $-ve$ DC bus</th>
<th>Output PWM voltage level</th>
<th>Combination No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{DC}$</td>
<td>$V_{DC}/3$</td>
<td>$2V_{DC}/3$</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>$V_{DC}$</td>
<td>0</td>
<td>$V_{DC}$</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>$2V_{DC}/3$</td>
<td>$V_{DC}/3$</td>
<td>$V_{DC}/3$</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>$2V_{DC}/3$</td>
<td>0</td>
<td>$2V_{DC}/3$</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>$2V_{DC}/3$</td>
<td>$V_{DC}/3$</td>
<td>$V_{DC}/3$</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>$2V_{DC}/3$</td>
<td>$2V_{DC}/3$</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>$V_{DC}/3$</td>
<td>$V_{DC}/3$</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>$V_{DC}/3$</td>
<td>$2V_{DC}/3$</td>
<td>$V_{DC}/3$</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>$V_{DC}/3$</td>
<td>$V_{DC}$</td>
<td>$-2V_{DC}/3$</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>$V_{DC}/3$</td>
<td>$2V_{DC}/3$</td>
<td>$-V_{DC}/3$</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>0</td>
<td>$V_{DC}$</td>
<td>$-V_{DC}$</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>0</td>
<td>$2V_{DC}/3$</td>
<td>$-2V_{DC}/3$</td>
<td></td>
</tr>
</tbody>
</table>
The simulation and experimental No - Load output voltage of 6 - Leg inverter are shown in Fig. 2.8 and Fig. 2.9 respectively.

Table 2.3: Specifications of Inverter

<table>
<thead>
<tr>
<th>SI.No.</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DC Bus voltage</td>
<td>12 V</td>
</tr>
<tr>
<td>2</td>
<td>Maximum output voltage</td>
<td>20 V pk-pk</td>
</tr>
<tr>
<td>3</td>
<td>Maximum output current</td>
<td>20 A pk-pk</td>
</tr>
<tr>
<td>4</td>
<td>Operating frequency</td>
<td>10 Hz $&lt;f_m&lt; 5.2$ kHz</td>
</tr>
<tr>
<td>5</td>
<td>Switching frequency</td>
<td>52 kHz</td>
</tr>
</tbody>
</table>

2.3 Switching device selection and Loss calculation

At lower voltage levels and high switching frequencies, MOSFETs have very less losses when compared to IGBTs. So it has been decided to use IRF3710 MOSFET as switching device. This device have 23 mΩ On-state resistance and the current carrying capability of 57 A. To reduce the losses much further, 3 devices are paralleled together. Totally each leg has 6
MOSFETs. So, each Unit contains 18 MOSFETs. Loss Calculation below is done for one device.

2.3.1 Conduction Loss

It has been assumed that the current is equally shared by all the 3 MOSFETs which are paralleled. This assumption is valid because MOSFETs have positive temperature coefficient. It means that in the parallel connection if one of them draws more current than others, its internal temperature will increase, this will increase its on-state resistance, to automatically reduce the current through it. Conduction losses of MOSFET and body diode of one switch in one leg is shown in equations (2.1) and (2.2) respectively.

\[
MOSFET\ Conduction\ Loss = \sum_{n=1}^{N} \frac{i_{ac}^2[n] \ast d[n] \ast R_{DS,on}}{f_s/f_m} \quad (2.1)
\]
\[
Diode\ Conduction\ Loss = \sum_{n=1}^{N} \frac{V_{FD} \ast i_{ac}[n] \ast (1 - d[n])}{f_s/f_m} \quad (2.2)
\]

where,

\[
i_{ac}[n] = Instantaneous\ current\ through\ single\ switch = I_{pk} \ast \sin(2\pi f_m T_s n - \phi)
\]
\[
d[n] = Modulation\ signal\ on\ unit\ scale = \frac{1 + m \ast \sin(2\pi f_m T_s n)}{2}
\]
\[
I_{pk} = Peak\ current\ through\ single\ switch
\]
\[
\phi = Phase\ difference\ between\ current\ and\ voltage
\]
\[
m = Modulation\ index\ (0.833 - maximum)
\]
\[
f_m = Modulation\ frequency / Operating\ frequency
\]
\[
f_s = Switching\ frequency
\]
\[
T_s = Switching\ time\ period, \frac{1}{f_s}
\]
\[
N = Number\ of\ samples\ in\ one\ cycle\ of\ modulation\ signal, \frac{f_s}{f_m}
\]
\[
R_{DS,on} = MOSFET\ on-state\ resistance, \ 23\ m\Omega\ (datasheet\ value)
\]
\[
V_{FD} = Diode\ forward\ voltage\ drop, \ 1.2\ V\ (datasheet\ value)
\]
2.3.2 Switching loss

Switching losses in device is mainly composed of MOSFET switching transition loss and diode reverse recovery loss. A buck chopper has been built to measure the switching times of the MOSFET with input voltage of 15 V and output current of 3 A at 50% duty cycle. It has been observed that the ON time of MOSFET is 100 ns and its OFF time is 500 ns. Switching losses of MOSFET and body diode of one switch in one leg is shown in equations (2.3) and (2.4) respectively. Diode switching transition losses are neglected because they are negligible compared to its reverse recovery loss.

\[
MOSFET \text{ Switching Loss} = \sum_{n=1, i_{ac}[n] \geq 0}^{N} \frac{V_{DC} \cdot i_{ac}[n] \cdot (t_{ON} + t_{OFF}) \cdot f_s}{6} \tag{2.3}
\]

\[
Diode \text{ Switching Loss} = \frac{1}{2} \cdot Q_{rr} \cdot V_{DC} \cdot f_s \tag{2.4}
\]

where,

\[
t_{ON} = \text{ ON time of MOSFET}
\]

\[
t_{OFF} = \text{ OFF time of MOSFET}
\]

\[
V_{DC} = \text{ DC Bus voltage}
\]

\[
Q_{rr} = \text{ Worst case reverse recovery charge of diode, 1010 nC (datasheet value)}
\]

2.3.3 Total loss

Worst case total losses of one Unit of the Inverter is calculated at different power factors and at extreme operating frequencies. These are listed in table 2.4. Also for comparison, total losses of Unit without interleaving is calculated at 5.2 kHz and listed in table 2.5. All the calculations are done in spread sheet. The following observations are deduced from loss calculations —

- Switching losses remain constant by variation in power factor
- Conduction losses increases with increase in power factor angle
- Last but not the least, total losses are reduced by 47% due to interleaving
Table 2.4: Unit losses with Interleaved carriers

<table>
<thead>
<tr>
<th>Operating frequency $f_m$</th>
<th>Power factor angle $\phi$</th>
<th>Conduction loss (Watts)</th>
<th>Switching loss (Watts)</th>
<th>Total loss (Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Hz</td>
<td>0°</td>
<td>1.9198</td>
<td>5.0579</td>
<td>6.9777</td>
</tr>
<tr>
<td></td>
<td>30°</td>
<td>2.1829</td>
<td>5.0579</td>
<td>7.2408</td>
</tr>
<tr>
<td></td>
<td>45°</td>
<td>2.4950</td>
<td>5.0579</td>
<td>7.5529</td>
</tr>
<tr>
<td></td>
<td>60°</td>
<td>2.9017</td>
<td>5.0579</td>
<td>7.9596</td>
</tr>
<tr>
<td></td>
<td>90°</td>
<td>3.8840</td>
<td>5.0579</td>
<td>8.9419</td>
</tr>
<tr>
<td>5.2 kHz</td>
<td>0°</td>
<td>1.5431</td>
<td>5.0163</td>
<td>6.5594</td>
</tr>
<tr>
<td></td>
<td>30°</td>
<td>1.7993</td>
<td>5.0766</td>
<td>6.8759</td>
</tr>
<tr>
<td></td>
<td>45°</td>
<td>2.0807</td>
<td>5.0879</td>
<td>7.1686</td>
</tr>
<tr>
<td></td>
<td>60°</td>
<td>2.4814</td>
<td>5.0854</td>
<td>7.5668</td>
</tr>
<tr>
<td></td>
<td>90°</td>
<td>3.3972</td>
<td>5.0733</td>
<td>8.4705</td>
</tr>
</tbody>
</table>

Table 2.5: Unit losses without Interleaved carriers ($f_m = 5.2 \text{ kHz}$)

<table>
<thead>
<tr>
<th>Power factor angle $\phi$</th>
<th>Conduction loss (Watts)</th>
<th>Switching loss (Watts)</th>
<th>Total loss (Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0°</td>
<td>4.6412</td>
<td>5.7055</td>
<td>10.3467</td>
</tr>
<tr>
<td>30°</td>
<td>5.3850</td>
<td>5.7317</td>
<td>11.1167</td>
</tr>
<tr>
<td>45°</td>
<td>6.2678</td>
<td>5.7289</td>
<td>11.9967</td>
</tr>
<tr>
<td>60°</td>
<td>7.4164</td>
<td>5.7227</td>
<td>13.1391</td>
</tr>
<tr>
<td>90°</td>
<td>10.1917</td>
<td>5.7229</td>
<td>15.9146</td>
</tr>
</tbody>
</table>

2.4 Heat sink thermal analysis

Heat sinks are used to operate the devices efficiently without exceeding their maximum junction temperatures. This section gives the thermal analysis of the heat sink with natural cooling. We will discuss how the heat sink thermal resistance depends on ambient temperature and finally mention the maximum power loss that can be dissipated from each switch at different ambient temperatures. The heat sink used in the experiment is the parallel plate-fin heat sink which is shown in Fig. 2.10. Its geometrical specifications are shown in table 2.6.
2.4. Heat sink thermal analysis

The heat transfer from heat sink to ambient is dominantly convective in nature. Hence, only convective thermal resistance is estimated. Convective thermal resistance depends on heat sink convective thermal coefficient and its geometry. In the determination of thermal coefficient, a dimensionless quantity called Nusselt number is used. Nusselt number is the function of velocity of fluid flow, the properties of the fluid medium and the geometry of the hot solid body which transfers the heat to the fluid [11]. In the case of natural cooling, we also require another dimensionless quantity called Rayleigh number. The following equations

![Figure 2.10: Parallel plate-fin heat sink](image)

<table>
<thead>
<tr>
<th>SI.No.</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Number of fins, $N_{fin}$</td>
<td>19</td>
</tr>
<tr>
<td>2</td>
<td>Width of base plate, $W$</td>
<td>193 mm</td>
</tr>
<tr>
<td>3</td>
<td>Height of fin, $H$</td>
<td>60 mm</td>
</tr>
<tr>
<td>4</td>
<td>Length of fin, $L$</td>
<td>300 mm</td>
</tr>
<tr>
<td>5</td>
<td>Thickness of fin, $t$</td>
<td>4 mm</td>
</tr>
<tr>
<td>6</td>
<td>Gap between adjacent plates, $b$</td>
<td>7 mm</td>
</tr>
</tbody>
</table>

Table 2.6: Specifications of Heat sink
are used to calculate the parallel plate-fin heat sink thermal resistance\textsuperscript{10}.

\[
Rayleigh \ number, \ R_a = \frac{g\beta(T_s - T_a)b^4}{\delta\vartheta L} \tag{2.5}
\]

\[
Nusselt \ number, \ N_u = \frac{R_a}{24} \left(1 - e^{-\frac{35}{R_a}}\right)^{0.75} \tag{2.6}
\]

\[
Heat \ transfer \ coefficient, \ h = \frac{N_u k}{b} \tag{2.7}
\]

\[
Heat \ sink \ thermal \ resistance, \ R_{\theta\text{sa}} = \frac{1}{h(A_{\text{base}} + N_{\text{fin}}A_{\text{fin}})} \tag{2.8}
\]

where,

\[
\beta = Coefficient \ of \ thermal \ expansion \ of \ air, \ 1/300^\circ K
\]

\[
g = Acceleration \ due \ to \ gravity, \ 9.81 \ m/s^2
\]

\[
\delta = Thermal \ diffusivity \ of \ air, \ 2.6 \times 10^{-5} \ m^2/s
\]

\[
\vartheta = Kinematic \ viscosity \ of \ air, \ 1.8 \times 10^{-5} \ m^2/s
\]

\[
k = Thermal \ conductivity \ of \ air, \ 0.028 \ W/\ ^\circ K/m
\]

\[
T_s = Heat \ sink \ temperature
\]

\[
T_a = Ambient \ temperature
\]

\[
A_{\text{base}} = Surface \ Area \ of \ base \ plate, \ W \times L
\]

\[
A_{\text{fin}} = Area \ of \ base \ plate, \ 2 \times H \times L
\]

Substituting the above parameters in equations (2.5), (2.6), (2.7) and (2.8) we get,

\[
R_{\theta\text{sa}} = 17.255 \frac{T_s - T_a}{T_s - T_a} \times \left(1 - e^{-\frac{68.85}{T_s - T_a}}\right)^{-0.75} \tag{2.9}
\]

The thermal model of the Unit considered for calculating the heat sink thermal resistance is shown in Fig. 2.11. From the datasheet of the device, we have maximum operating junction temperature, \(T_j\) as 175\(^\circ\)C. But for safety of device let us allow maximum operating junction temperature to 130\(^\circ\)C. Junction to casing thermal resistance, \(R_{\theta\text{jc}}\) is given as 0.75\(^\circ\)C/W. Casing to sink thermal resistance, \(R_{\theta\text{cs}}\) depends on heat sink compound used and the thermal conductive material placed between device and heat sink. Its value is 0.50\(^\circ\)C/W. From the
2.4. Heat sink thermal analysis

thermal model of the Unit shown in Fig. 2.11 at 130°C junction temperature we have,

\[ 18 \times \left( \frac{130 - T_s}{1.25} \right) = \frac{T_s - T_a}{R_{\theta sa}} \]  \hspace{1cm} (2.10)

From equations (2.9) and (2.10), we can get heat sink temperature, \( T_s \) and heat sink thermal resistance, \( R_{\theta sa} \) at different ambient temperatures, when the junction temperature is 130°C. At an ambient temperature of 45°C, thermal resistance of heat sink is 0.34788°C/W. Hence, from the thermal model of Unit, maximum power loss per switch can be 11.315 W. The variation of heat sink thermal resistance and maximum allowable power loss per switch with ambient temperature at operating junction temperature of 130°C is shown in Fig. 2.12 and Fig. 2.13 respectively.

Following conclusions can be made from the graphs —

- Heat sink thermal resistance increases with ambient temperature
- Maximum allowable power loss of the inverter can more when the low ambient temperatures are maintained
- Power rating of the inverter can be increased by forced cooling
Figure 2.12: Heat sink thermal resistance Versus Ambient temperature

Figure 2.13: Maximum allowable power loss per switch Versus Ambient temperature
2.5 Design of dc bus capacitance

The function of dc bus capacitance is to take the ripple current consisting of double frequency component and switching frequency component while maintaining ripple voltage to be very small. Here double frequency component is the component which is double the operating frequency / modulation frequency. The design of dc bus capacitance depends on the rms current calculation and its correlation with the voltage ripple.

2.5.1 Calculation of double frequency component ripple

All the calculations are done for worst case conditions of 20 A peak-peak output current and 20 V peak-peak output voltage. Double frequency component is evaluated by considering power balance. That is,

\[
V_{DC} \times i_{DC}(t) = v_{ac}(t) \times i_{ac}(t) \]  

(2.11)

\[ \Rightarrow i_{DC}(t) = \frac{v_{ac}(t) \times i_{ac}(t)}{V_{DC}} \]  

(2.12)

\[ \Rightarrow i_{DC}(t) = \frac{v_{ac,m} \times i_{ac,m} \times \sin(\omega t) \times \sin(\omega t - \phi)}{V_{DC}} \]  

(2.13)

\[ \Rightarrow i_{double \ frequency} = \frac{-v_{ac,m} \times i_{ac,m} \times \cos(2\omega t - \phi)}{2V_{DC}} \]  

(2.14)

where,

- \( v_{ac,m} \) = Amplitude of output voltage of inverter
- \( i_{ac,m} \) = Amplitude of output current of inverter
- \( \phi \) = Phase angle between \( v_{ac}(t) \) and \( i_{ac}(t) \)

Substituting the required inverter specifications in equation (2.14), the rms double frequency current component is obtained as,

\[ i_{double\ frequency,\ rms} = 2.946 \ A \]
2.5.2 Calculation of switching frequency ripple

The DC bus current waveform helps in the calculation of switching frequency ripple. Capacitor ripple current waveform due to the switching action of Unit I alone is shown in Fig. 2.14(b). Fig. 2.14(c) and (d) shows the switches which are ON when the Unit is operating in blue and pink shaded bands of Fig. 2.14(a) respectively, when the modulating signal is in region 1. ON state switch is shown with the colour corresponding to the band shade of operating region.

Similarly, the capacitor current due to switching action of Unit II alone can also be obtained. The total DC bus current is obtained by summation of the capacitor current due to switching of Unit I and Unit II, which is shown in Fig. 2.15. The waveform in Fig. 2.15(d) is also equal to summation of DC bus currents due to three H-bridges, whose carrier waves are phase shifted by 120°. Hence, without much loss of accuracy, we can calculate high frequency capacitor ripple current due to one H-bridge and multiply by $\sqrt{3}$ to get total DC bus capacitor ripple current. High frequency capacitor ripple current due to single H-bridge configuration is given by equation (2.15).

\[
i_{\text{high frequency, rms}} = \sqrt{\frac{1}{N} \sum_{n=1}^{N} i_{L1}^2[n] \{|D_I - D_{II}| - (D_I - D_{II})^2\}}
\]  

(2.15)

where,

\[D_I = 0.5 + 0.333 \sin(\omega t) = \text{Modulation signal of Unit I}\]
\[D_{II} = 0.5 - 0.333 \sin(\omega t) = \text{Modulation signal of Unit II}\]
\[N = \frac{f_m}{f_s}\]
\[T_s = \frac{1}{f_s}\]
\[i_{L1}[n] = \text{Instantaneous load current due to single H-bridge} = I_{L1(pk)} * \sin(2\pi f_m T_s n - \phi)\]

A comparison between the DC bus ripple current magnitudes at different power factors with a modulation frequencies of 10 Hz and 5.2 kHz, due to classical H-bridge topology and 6-leg topology is shown in table 2.7. Looking at the comparison table we can conclude that the high frequency DC bus capacitor ripple current is reduced by 42% due to interleaving of carriers. Net DC bus ripple current is given by,

\[
i_{\text{cap, ripple}} = \sqrt{i_{\text{double frequency, rms}}^2 + i_{\text{high frequency, rms}}^2}
\]  

(2.16)
2.5. Design of dc bus capacitance

Figure 2.14: (a) Bands showing 2 different operating states of Unit I (b) Capacitor current due to switching of Unit I (c) ON state switches of Unit I in blue shaded band (d) ON state switches of Unit I in pink shaded band
Figure 2.15: (a) Carrier signals and modulation signals of Inverter (b) Capacitor current due to switching of Unit I (c) Capacitor current due to switching of Unit II (d) Total DC bus capacitor current
2.5. Design of dc bus capacitance

<table>
<thead>
<tr>
<th>Operating frequency</th>
<th>Power factor angle</th>
<th>High frequency ripple current with interleaving (A)</th>
<th>High frequency ripple current without interleaving (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0°</td>
<td>1.9198</td>
<td>3.4099</td>
</tr>
<tr>
<td></td>
<td>30°</td>
<td>1.9687</td>
<td>3.2967</td>
</tr>
<tr>
<td></td>
<td>45°</td>
<td>1.9034</td>
<td>3.1796</td>
</tr>
<tr>
<td></td>
<td>60°</td>
<td>1.7655</td>
<td>3.0579</td>
</tr>
<tr>
<td></td>
<td>90°</td>
<td>1.6923</td>
<td>2.9311</td>
</tr>
<tr>
<td>10 Hz</td>
<td>0°</td>
<td>1.9642</td>
<td>3.4098</td>
</tr>
<tr>
<td></td>
<td>30°</td>
<td>1.9164</td>
<td>3.2996</td>
</tr>
<tr>
<td></td>
<td>45°</td>
<td>1.8675</td>
<td>3.1857</td>
</tr>
<tr>
<td></td>
<td>60°</td>
<td>1.8172</td>
<td>3.0674</td>
</tr>
<tr>
<td></td>
<td>90°</td>
<td>1.7656</td>
<td>2.9445</td>
</tr>
<tr>
<td>5.2 kHz</td>
<td>0°</td>
<td>1.9642</td>
<td>3.4098</td>
</tr>
<tr>
<td></td>
<td>30°</td>
<td>1.9164</td>
<td>3.2996</td>
</tr>
<tr>
<td></td>
<td>45°</td>
<td>1.8675</td>
<td>3.1857</td>
</tr>
<tr>
<td></td>
<td>60°</td>
<td>1.8172</td>
<td>3.0674</td>
</tr>
<tr>
<td></td>
<td>90°</td>
<td>1.7656</td>
<td>2.9445</td>
</tr>
</tbody>
</table>

Its worst case value is calculated as,

\[ i_{cap \, \text{ripple, worst case}} = 3.543 \, \text{A} \]

100 V, 470 \mu F capacitors with a ripple current capability of 1.6 A at frequency of 156 kHz is chosen. 156 kHz frequency is chosen because switching ripple frequency is 3 times the switching frequency of MOSFETs. Each unit has 16 capacitors connected in parallel to limit the double frequency ripple voltage below 20% at worst case conditions, as the voltage ripple is mainly due to double frequency current component. Hence, total number of DC bus capacitors connected in parallel for the 6-Leg inverter is 32. The double frequency capacitor voltage ripple is given by equation (2.17).

\[ \Delta V = \frac{i_{\text{double frequency, peak}}}{4\pi f_m C} \quad (2.17) \]

Worst case voltage ripple occurs at low modulating frequency. Double frequency voltage ripple at modulating frequency of 10 Hz is evaluated as 2 V peak-peak, which is 16% of DC bus voltage. Hence, the capacitor value is adequate.
Chapter 2. Topology of the Amplifier and its Design

2.6 Phase Shifted Carrier (PSC) generation

Generation of phase shifted carriers can be done in either digital domain or analog domain. Clock frequency of the present digital controllers is the bottle neck to generate high frequency triangular waves of good resolution and sufficient amplitude. Whereas, square waves of high frequency can be generated easily in digital controller, since it involves only toggling of output pins. Hence, an analog circuit has been designed to generate high frequency phase shifted carriers, which takes the square waves as input from the digital controller. The block diagram of PSC generation circuit is shown in Fig. 2.16.

\[\text{Figure 2.16: Block diagram of Phase Shifted Carrier generation circuit}\]

The PSC generation circuit has an integrator which integrates the square wave from digital controller to get the triangular wave. But the practical integrators built using Operational Amplifiers saturates due to the bias voltages at the input terminals. Hence, a low pass filter is used to extract the DC component present in the output of an integrator, which is then subtracted from the input square wave. This principle generates the clean triangular waves with zero offset. The filter used should have minimum phase shift to avoid the problem of instability. Integrator with large time constant acts as low pass filter with minimum phase shift\[9\]. So, even in the place of low pass filter shown in Fig. 2.16, an integrator with very large time constant is used.

2.6.1 Analog circuit for PSC generation and its stability analysis

The PSC generation circuit is shown in Fig. 2.17. Integrator built using Op-Amp 2 acts as low pass circuit. This integrator extracts the inverted DC component present in the output \(V_o\). Hence, its output is given as input to the Op-Amp 1 at the non - inverting terminal. The input - output relations of Op-Amp 1 and Op-Amp 2 are given by equations (2.18) and
2.6. Phase Shifted Carrier (PSC) generation

Figure 2.17: Circuit diagram of Phase Shifted Carrier generator

From equations (2.18) and (2.19) we have,

\[ V_o(t) + \frac{1}{R_1 C_1} \int V_c(t) \, dt - \frac{1}{R_1 C_1} \int V_i(t) \, dt = 0 \quad (2.20) \]

Differentiating equation (2.20) twice we get,

\[ \frac{d^2 V_o(t)}{dt^2} + \frac{1}{R_2 C_2} \frac{dV_o(t)}{dt} + \frac{1}{R_1 R_2 C_1 C_2} \int V_o(t) \, dt + \frac{1}{R_1 C_1} \int V_i(t) \, dt = 0 \quad (2.21) \]

Applying Laplace transform to equation (2.21) and rearranging the terms we get,

\[ \frac{V_o(s)}{V_i(s)} = \frac{-\frac{s}{R_1 C_1}}{s^2 + \frac{s}{R_2 C_2} + \frac{1}{R_1 R_2 C_1 C_2}} \quad (2.22) \]

The poles of transfer function shown in equation (2.22) are always on left half of s-plane. Hence, the system is stable.
Chapter 2. Topology of the Amplifier and its Design

The detailed block diagram of the system can be drawn using equations (2.18) and (2.19) after applying Laplace transform to them. This is shown in Fig. 2.18. With $R_1 = 80$ KΩ, $R_2 = 1$ MΩ, $C_1=1$ nf and $C_2=10$ nf, the Bode plot of open loop transfer function of the system is shown in Fig. 2.19. The phase margin is about 6°, confirming the practical system to be stable.

Figure 2.18: Detailed block diagram of Phase Shifted Carrier generation circuit

Figure 2.19: Bode plot of open loop transfer function of PSC generation circuit

Detailed schematics of the Phase shifted carrier generation circuit with addition features for advanced modulation techniques is shown in Appendix.
2.6.2 Sequential circuit implementation in FPGA

To generate phase shifted carriers, we need phase shifted square waves. These are generated in FPGA digital controller, the details of which are given in Chapter 4. Fig. 2.20(b) shows the state diagram for 120° phase shifted square waves shown in Fig. 2.20(a). But this is not self starting state diagram. To make it self starting, other two states, 111 and 000 are also included in the state diagram shown in Fig. 2.20(c). The state table using D-flip flops for the self starting state diagram is shown in table 2.8.

![State diagram for 3-phase square wave generation](image)

Figure 2.20: State diagram for 3-phase square wave generation
Table 2.8: State table for generation of 120° phase shifted square waves

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
<th>Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1^n$</td>
<td>$Q_2^n$</td>
<td>$Q_3^n$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

The equations for the inputs to D-flip flops are given by equations (2.23), (2.24) and (2.25) which are obtained using K-map. The clock frequency of D-flips flops is decided by the frequency of phase shifted carriers. Clock frequency can be reduced by using up counters and comparators. Phase shifts other than 120° between the carriers can also be obtained in the similar way.

\[
D_1 = \overline{Q_2} + Q_1Q_2 \tag{2.23}
\]
\[
D_2 = (Q_1 + Q_2)Q_3 \tag{2.24}
\]
\[
D_3 = \overline{Q_1} + Q_2Q_3 \tag{2.25}
\]

### 2.6.3 Features of PSC generation board

The following are the features of PSC generation board —

- Generates low distortion triangular carrier signals up to 400 kHz frequency
- Adjustable peak - peak amplitude of carrier signals with a maximum value of 24 V
- Adjustable offsets in the carriers to implement sine - triangle PWM for Multi-level inverters
- 6 channels with an option to give same or different modulation signals to each channel
- On board comparator for PWM pulse generation
2.6.4 Testing of PSC generation board

PSC generation board has been tested up to frequency of 416 kHz by giving a square wave from the function generator. Also, sine - triangle PWM has been implemented with a modulating signal of 50 Hz and carrier frequency of 1.6 kHz for the purpose of testing. Practical waveforms are shown in Fig. 2.21 and Fig. 2.22 respectively.

Figure 2.21: Carrier signal of frequency 416 kHz from PSC generation board - 5 V/div

Figure 2.22: Sine - triangle PWM — CH1(Green, 1 V/div): Sinusoidal modulation signal of frequency 50 Hz; CH2(Blue, 1 V/div): Triangular carrier signal of frequency 1.6 kHz; CH3(Pink, 20 V/div): PWM Pulses of 1.6 kHz

Phase shifted square wave signal from FPGA controller and phase shifted carrier waves at frequency of 52kHz are shown in Fig. 2.23 and Fig. 2.24 respectively.
2.7 Auxiliary circuits of Inverter

Different auxiliary circuits of Inverter include Gate drive cards, Protection and delay cards, Current and voltage sensing cards. All these auxiliary circuits design existed beforehand\cite{12}. These cards are tested sequentially for their working.

2.7.1 Protection and Delay card

The protection and delay card provides the complementary delayed PWM signals for the bottom switches of inverter by taking the PWM signals for top switches from PSC generation board. It also provides different protections to inverter like over-voltage protection, under-
2.8. Conclusion

This chapter discussed in detail about the working of 6-Leg inverter. It explained about the design of DC bus capacitor and how the switching device is selected. We also dealt with thermal analysis of heat sink and estimated the maximum allowable power loss per switch at different ambient temperatures. It even focussed on the phase shifted carrier generation in analog domain. In the end, it briefly discussed about auxiliary circuits of the inverter and how they have been used to achieve different objectives of the project.

voltage protection, over-current protection and DC bus short circuit protection. This board generates 12 PWM signals for the 12 switches in the 6 - Leg inverter.

2.7.2 Gate drive cards

The gate drive card is used mainly to provide the necessary gate current required by the MOSFETs. In this project, it is also used to provides an isolation between the Network analyzer and the inverter through the gate drive optocoupler HCPL-3101. This optical isolation makes it possible to test high power DUT that may be grounded or floating up to a voltage level of 600 V.

2.7.3 Current sensing cards

Current sensing cards are used to sense the load current. This sensed load current is used to implement the closed loop control to limit the output current from Inverter. The current sensing card used has has a low profile Hall effect current transformer HTP50, which can measure the currents in the range of $\pm 50$ A. It has a bandwidth of 100 kHz.

2.8 Conclusion

This chapter discussed in detail about the working of 6-Leg inverter. It explained about the design of DC bus capacitor and how the switching device is selected. We also dealt with thermal analysis of heat sink and estimated the maximum allowable power loss per switch at different ambient temperatures. It even focussed on the phase shifted carrier generation in analog domain. In the end, it briefly discussed about auxiliary circuits of the inverter and how they have been used to achieve different objectives of the project.
Chapter 3

Output Filter Design and Circulating Current Mitigation

3.1 Introduction

The output voltage of an inverter is rich with harmonics at switching frequency and its multiples. This voltage cannot be given directly to the load since the current drawn by the load will also have harmonics. Hence, generally a passive filter will be used to filter out the harmonics in output voltage and current of inverter. Different passive filters used in practice are L filter, LC filter and LCL filter depending on the application. In this project, only L filter is used as an output filter.

Multi leg inverters have a serious issue of circulating currents. These circulating currents are due to switching ON of both top and bottom switches of different legs during the modulation. These circulating currents are differential mode components of load current. Hence, a differential mode filter is designed to mitigate the circulating currents. This chapter explains in detail about different filters used in the experiment.

3.2 Design of L filter

3.2.1 Calculation of filter inductance

The value of inductor is calculated based on the voltage drop across it. 10 % - 15 % voltage drop across the filter inductor is generally acceptable. Equivalent circuit of one H-bridge in the 6-Leg inverter is shown in Fig. 3.1. The drop in the filter inductor is maximum at highest operating frequency. With the worst case conditions of load, considering 10 %
voltage drop at 5.2 kHz, the value of filter inductor for each H-bridge is obtained as 9.4 µH. In the experiment, we used 6 µH inductor for each leg of a unit as shown in Fig. 2.1 to avoid DC bus short circuit. This means that for each H-bridge we have 12 µH filter inductance. This causes a voltage drop of 13% which is in acceptable limits.

\[ \text{Figure 3.1: Average model of one H-bridge in 6-Leg inverter} \]

### 3.2.2 Design procedure

For the fabrication of inductor, several methods have been discussed in literature[7]. Area Product approach has be chosen to fabricate the filter inductor in this project. The design steps for fabrication are listed below —

- Calculate the energy stored in the inductor

\[ E = \frac{1}{2} LI_m^2 \]

where \( I_m \) is the peak inductor current

- Compute the Area Product and choose the core from core table with area product greater than or equal to \( A_p \)

\[ A_p = A_w A_c = \frac{2E}{K_w K_c J B_m} \]

where,

- \( A_w \) is the window area of core
- \( A_c \) is the core cross section area
- \( J \) is current density of copper wire — 2.5 A/mm²
3.2. Design of L filter

$B_m$ is the flux density — 0.2T for ferrite core

$K_w$ is the winding factor — 0.4 for multi layer winding

$K_c$ is the crest factor defined as ratio of peak current to rms current

- Calculate the number of turns

$$N = \frac{LI_m}{A_c B_m}$$

- Determine the gauge of wire

$$a_w = \frac{I_{\text{rms}}}{J}$$

choose the gauge of wire from wire table with wire cross section area greater than or equal to $a_w$

- Check whether the inequality, $A_w K_w > a_w N$ is satisfied. If not satisfied choose next bigger core and repeat the calculations.

- Calculate the air gap length

$$l_g = \frac{\mu_0 N^2 A_c}{L}$$

6 $\mu$H inductors have been designed following the above steps. The details of designed filter inductor is shown in table 3.1.

<table>
<thead>
<tr>
<th>SI.No.</th>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Current rating</td>
<td>14 A</td>
</tr>
<tr>
<td>2</td>
<td>Operating frequency</td>
<td>10 Hz $&lt; f_m &lt; 5.2$ kHz</td>
</tr>
<tr>
<td>3</td>
<td>Core material</td>
<td>Ferrite</td>
</tr>
<tr>
<td>4</td>
<td>Core number</td>
<td>EE 42/21/9</td>
</tr>
<tr>
<td>5</td>
<td>Conductor material</td>
<td>Copper</td>
</tr>
<tr>
<td>6</td>
<td>Wire gauge</td>
<td>19 SWG</td>
</tr>
<tr>
<td>7</td>
<td>Number of conductors</td>
<td>5</td>
</tr>
<tr>
<td>8</td>
<td>Number of turns</td>
<td>6</td>
</tr>
<tr>
<td>9</td>
<td>Air gap</td>
<td>0.8 mm</td>
</tr>
</tbody>
</table>
3.3 Circulating currents in Parallel inverters

It is desirable that each leg of the inverter carries a current which is one-third of load current. But in practice it is not possible due to circulating current (referred to as cross-current). Circulating currents are due to simultaneous turning ON of both top and bottom switches of different legs of a Unit during modulation. These circulating currents are the result of interleaving of carriers. Interleaving can make the magnitude of these currents worse if no precautions are taken.

Many methods have been discussed in literature to mitigate the circulating currents in 3-φ parallel inverters. Since in 3-φ inverters we have line currents summing up to zero, a common mode inductor built using toroidal core can be used to limit the cross current from one inverter to the other. Whereas, in case of single phase inverters, circulating currents are differential mode components of Leg currents. This makes the structure of the inductor complex as it demands the core with multiple limbs.

In this project, we have came up with a design of differential mode inductor which is less complex in structure and can be used for any number of legs in parallel single phase inverters. This inductor is built using simple ETD cores which are abundantly available. This section explains in detail about the concept and design principle of Differential Mode Inductor(DMI).

3.3.1 Concept of Differential Mode Inductor

![Diagram of Differential Mode Inductor](image)

Figure 3.2: (a) Structure of Differential mode inductor (b) Circuit Symbol

A simple differential mode inductor and its symbol is shown in Fig. 3.2. Here, common
mode current paths are a-b-e and c-d-e and differential mode current path is a-b-d-c. By using the right hand rule principle, we can get the direction of fluxs in the core due to both the currents which are shown by different colours. We can clearly see that the flux due to common mode current sum to zero when the current in the paths a-b-e and c-d-e are equal. Whereas, we have non-zero flux in the core, for the circulating current flowing through the path a-b-d-c. This implies that the inductor is effective only for the circulating current but not for the common mode current.

3.3.2 DMI design for 3-Leg half bridge inverter

![Diagram of DMI design for 3-Leg half bridge inverter](image)

Figure 3.3: Structure of DMI for 1-φ parallel half bridge inverters

The structure of the differential mode inductor designed for single phase parallel half bridge inverters is shown in Fig. 3.3 where \( i_a \), \( i_b \) and \( i_c \) are the Leg currents. Here circulating
currents are defined as

\[ i_{cc,ab} = 0.5(i_a - i_b) \] \hspace{1cm} (3.1)

\[ i_{cc,bc} = 0.5(i_b - i_c) \] \hspace{1cm} (3.2)

\[ i_{cc,ca} = 0.5(i_c - i_a) \] \hspace{1cm} (3.3)

where,

\[ i_{cc,ab} = \text{circulating current from Leg} - a \text{ to Leg} - b \]

\[ i_{cc,bc} = \text{circulating current from Leg} - b \text{ to Leg} - c \]

\[ i_{cc,ca} = \text{circulating current from Leg} - c \text{ to Leg} - a \]

In the Fig. 3.3 each core has 2 inductors wound on it. So, each of the above defined circulating currents pass through four inductors. The effective inductance for the circulating current is given by equation (3.4).

\[ L_{eff} = 4L \] \hspace{1cm} (3.4)

The value of \( L \) is evaluated using Faraday’s equation \( V = L \frac{di}{dt} \) and is given by equation (3.5).

\[ L = \frac{V_{DC} \Delta t}{4 \Delta i} \] \hspace{1cm} (3.5)

where,

\( L \) = Inductance of Inductor on each limb

\( \Delta i \) = Peak – peak circulating current

\( \Delta t \) = Effective switching time = \( \frac{1}{3f_s} \)

\( V_{DC} \) = DC bus voltage

The value of \( L \) for limiting the circulation current to 5% of load current is evaluated as 54 \( \mu \)H using equation (3.5). In the experiment we designed the inductor of value 60 \( \mu \)H. The fabrication of differential mode inductor is done using Area Product approach which is discussed previously. The value of \( I_m \) in the design steps is the amplitude of circulating current but not the amplitude of load current. This is because only circulating current causes the DMI to saturate. This principle makes the DMI to be compact in size.

The fabrication of differential mode inductor is done using ETD ferrite cores. 2 inductors are wound on each core with bifilar winding structure. The gauge of the conductor is decided
by the maximum load current. Table 3.2 shows the specifications of the differential mode inductor. The core number to be used based on calculations is ETD 30. Since this core do not have sufficient window area, we have chosen ETD 44 core.

### 3.4 Conclusion

This chapter discussed in detail about the output filter design using Area Product approach. It also focussed on the cause of circulating currents in the parallel inverters and their mitigation using passive differential mode filter. The concept of Differential Mode Inductor is explained and its application to single phase inverters is discussed.

<table>
<thead>
<tr>
<th>SI.No.</th>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Current rating</td>
<td>14 A</td>
</tr>
<tr>
<td>2</td>
<td>Operating frequency</td>
<td>156 kHz</td>
</tr>
<tr>
<td>3</td>
<td>Core material</td>
<td>Ferrite</td>
</tr>
<tr>
<td>4</td>
<td>Core number</td>
<td>ETD 44</td>
</tr>
<tr>
<td>5</td>
<td>Conductor material</td>
<td>Copper</td>
</tr>
<tr>
<td>6</td>
<td>Wire gauge</td>
<td>19 SWG</td>
</tr>
<tr>
<td>7</td>
<td>Number of conductors</td>
<td>10</td>
</tr>
<tr>
<td>8</td>
<td>Number of turns</td>
<td>5</td>
</tr>
<tr>
<td>9</td>
<td>Air gap</td>
<td>0.1 mm</td>
</tr>
</tbody>
</table>
Chapter 4

Closed Loop Control Design

4.1 Introduction

The output current of an inverter depends on load. There will be nothing to prevent the current drawn by the load from the inverter. This will damage the inverter or trip it when the protection is given, causing interruptions during the process of characterization of device. Hence, a closed loop controller is to be designed to limit the current. Also, when the current is below the reference limit, output voltage of the inverter should be maintained at specification value. So, the controller designed should work in both voltage mode control and current mode control depending on the conditions of load. This chapter discusses the control principle used and how different control blocks are implemented in digital controller.

4.2 Digital controller

FPGA based digital platform is used for the closed loop control. The choice of an FPGA device for a given application is based on the number of logic elements required, clock speed and number of I/O pins. ALTERA EP1C12Q240C8 was found to be suitable for this application. The board was programmed using Quartus II (Version 9.1) software.

4.2.1 FPGA board

The block diagram of the FPGA digital controller board is shown in Fig. 4.1. The devices interfaced with the FPGA chip include configuration device (EEPROM), ADC and DAC. General purpose I/O pins are also available on the board which can be used to synchronize different external devices. The FPGA has logic elements arranged in rows and columns.
The vertical and horizontal interconnects of varying speeds provide signal interconnects to implement the custom logic. Each logic element has certain hardware resources which will be utilised by the routing software to realize the user logic. The device data is furnished in table 4.1.

### 4.2.2 ADC

AD7864AS-1 of analog devices is the ADC chip present on the FPGA platform. It is used to convert the analog input signals from the system into digital signals which are used for further processing. This 12-bit, 44-pin simultaneous sampling ADC has 4 channels with a conversion time of 1.6 $\mu$s per channel. There are 4 such ADCs on the board and hence can take up to 16-analog inputs.

### 4.2.3 DAC

AD5447 of analog devices is the DAC present on the FPGA platform. It is used to convert the digital data from the controller into analog data. This 12-bit, 24-pin, dual channel, current output DAC has a conversion time of 10$\mu$s.
4.3 Block diagram of the controller

Many closed loop controllers are discussed in literature for 3-φ and 1-φ inverters in which the output current of inverter is always maintained constant even if the load is increased. All these control techniques use either PI controller for 3-φ inverters or PR controller for 1-φ inverters. Moreover, these control laws work only at a particular operating frequency of inverter. In the present application, the operating frequency of the inverter varies and also the load is not known. This makes the design of controller for the present application quite challenging.

The sweep rate of the sweep signal from the network analyzer is low. This means that, the controller designed need not have high bandwidth. Also, the output current of inverter can be varied by varying the modulation index of modulation signal. Using these 2 facts, the controller for the present application is designed. The block diagram of the closed loop controller is shown in Fig. 4.2. The controller will calculate the peak levels of modulation voltage, $V_{\text{modulation}}$, and sensed output current, $I$, of the inverter using Peak detector blocks. Depending on the peak values of modulation voltage and output current, the sequential circuit block decides whether to scale down the sweep signal or to scale up using the up / down counter. The counter gain varies only from 0 to 1. The counter gain is multiplied

---

**Table 4.1: Specifications of ALTERA FPGA device**

<table>
<thead>
<tr>
<th>SI.No.</th>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Part Number</td>
<td>EP1C12Q240C8</td>
</tr>
<tr>
<td>2</td>
<td>Manufacturer</td>
<td>Altera</td>
</tr>
<tr>
<td>3</td>
<td>Number of pins</td>
<td>240</td>
</tr>
<tr>
<td>4</td>
<td>Number of I/O pins</td>
<td>60</td>
</tr>
<tr>
<td>5</td>
<td>Package</td>
<td>PQFP</td>
</tr>
<tr>
<td>6</td>
<td>Number of logic elements</td>
<td>12,080</td>
</tr>
<tr>
<td>7</td>
<td>Number of PLLs</td>
<td>2</td>
</tr>
<tr>
<td>8</td>
<td>Maximum clock frequency using PLL</td>
<td>275 MHz</td>
</tr>
<tr>
<td>9</td>
<td>Power supply required for core</td>
<td>1.5 V (VCCINT)</td>
</tr>
<tr>
<td>10</td>
<td>Power supply required for I/O</td>
<td>3.3 V (VCCIO)</td>
</tr>
<tr>
<td>11</td>
<td>Power supply required for PLL circuit</td>
<td>1.5 V (VCCPLL)</td>
</tr>
</tbody>
</table>
to sweep signal for scaling it. Here, the sequential circuit block is the one which decides whether the controller has to operate in voltage control mode or current control mode. Implementation of different blocks in FPGA is discussed in detail in the next section.

4.4 Digital implementation of control blocks

4.4.1 Peak detector

DQ transformation is a very popular technique used in the design of controller for 3-φ inverters to obtain the peak values of sinusoidal voltages and currents. This technique can also be used in 1-φ systems by delaying the sine wave by 90° to obtain the quadrature component. Here, a PLL is needed to track the frequency of sine wave whose design parameters depend on frequency of the sine wave to be tracked. Hence, we cannot use this method in the present application since the operating frequency of the inverter varies continuously.

The peak detector designed in this project can give the peak value of any periodic waveforms having the zero crossing. Without the zero crossing the designed peak detector does not work. This is not an issue since the output voltage and current of the inverter will always have zero crossing. The waveforms shown in Fig. 4.3 will be helpful to understand the design of peak detector.
4.4. Digital implementation of control blocks

Figure 4.3: Timing diagram and related waveforms of the Peak detector
Consider the waveform \( y[n] \) in the Fig. 4.3. This signal is the digital equivalent of the analog signal given as input to ADC. \( x[n] \) is the waveform which is obtained after processing \( y[n] \) by using the digital circuit shown in Fig. 4.4. In the circuit shown in Fig. 4.4, the D-flip flop gives \( y[n-1] \) signal as its output when clock signal is given continuously. Since \( x[n] \) follows \( y[n] \) from 0° to 90°, the clock signal to the D-flip flop should be given only in this interval. In this interval, \( y[n] > 0 \) and \( y[n] > y[n-1] \). The condition \( y[n] > y[n-1] \) is obtained using the comparator-(a>b). The condition \( y[n] > 0 \) is accomplished using the circuit shown in Fig. 4.5(b) whose output \( b[n] \) is one of the inputs to AND gate-2 in Fig. 4.4. The output of AND gate-2 is used to enable the clock to D-flip flop. The clock signal to D-flip flop is shown as Tracking clk signal in Fig. 4.3.

From the \( x[n] \) waveform, it is clear that except in the interval 0° - 90°, the peak value of first cycle is obtained. But, if the magnitude of \( y[n] \) decreases, the \( x[n] \) waveform remains at the peak of previous cycle. So, it should be reset at starting of every cycle. This is done by the asynchronous clear input \( p[n] \) to D-flip flop. \( p[n] \) signal is obtained using the circuit shown in Fig. 4.6(a). If we sample the waveform \( x[n] \) at negative zero crossing of \( y[n] \) using a D-flip flop, then we obtain the peak value of \( y[n] \). This is done by the circuit shown in Fig. 4.7. \( q[n] \) is the output of the circuit shown in Fig. 4.6(b). The input \( b[n] \) in the circuit shown in Fig. 4.6(b) is obtained from the output of comparator-(\( y[n] > 0 \)) of Fig. 4.5(b).
4.4. Digital implementation of control blocks

Figure 4.5: (a) Digital circuit to obtain $y[n]<0$ (b) Digital circuit to obtain $y[n]>0$

Figure 4.6: (a) Digital circuit to obtain a pulse at positive zero crossing (b) Digital circuit to obtain a pulse at negative zero crossing

Figure 4.7: Sampling circuit to obtain Peak value of $y[n]$
4.4.2 Current / Voltage mode decisive circuit

Current / Voltage mode decisive circuit is the sequential circuit block shown in Fig. 4.1. This circuit decides the value of up / down counter to scale the sweep signal from Network analyzer. This circuit takes the peak values of modulation signal and output current to decide whether the counter has to count up or down. Table 4.2 shows the truth table for the operation of this circuit.

Table 4.2: Truth table of Current / Voltage mode decisive circuit

<table>
<thead>
<tr>
<th>$V_{\text{peak}}$</th>
<th>$I_{\text{peak}}$</th>
<th>up / down</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

In the truth table, if the actual quantity is greater than the reference value, it is entered as 1. This truth table is same as the truth table for NOR gate. The Current / Voltage mode decisive circuit is shown in Fig. 4.8.

Figure 4.8: Current / Voltage mode decisive circuit

The above circuit even takes care of soft start of the total system. The bandwidth of the controller is decided by the clock frequency of the clock signal given to up/down counter.

4.4.3 Per-unit Values

All the control blocks are implemented in 16-bit digital arithmetic. The per-unit values and the equivalent hex code are listed in table 4.3.
4.5 Conclusion

This chapter discussed about the limitations of conventional controllers in the present application and explained a control strategy which can work in both voltage mode control and current mode control. It discussed in detail about the implementation of different control blocks in digital controller.
Chapter 5

Simulation and Experimental Results

5.1 Introduction

This chapter presents the simulation results of the open loop operation of 6-Leg inverter. It also presents the Experimental results of the closed loop system at different frequencies. In the experiment carried out, the load of the inverter is chosen to be inductor of value 750 µH.

5.2 Simulation results

Simulation of the 6-Leg inverter is done in MATLAB 7.0 to check the output voltage, load current and circulating currents and validate the design values. The parameters used in simulation are listed in table 5.1.

<table>
<thead>
<tr>
<th>SI. No.</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Modulation frequency</td>
<td>5.2 kHz</td>
</tr>
<tr>
<td>2</td>
<td>Switching frequency</td>
<td>52 kHz</td>
</tr>
<tr>
<td>3</td>
<td>Filter Inductance</td>
<td>6 µH</td>
</tr>
<tr>
<td>4</td>
<td>Differential Mode Inductor</td>
<td>60 µH</td>
</tr>
<tr>
<td>5</td>
<td>DC bus capacitor</td>
<td>15 mF</td>
</tr>
<tr>
<td>6</td>
<td>DC bus voltage</td>
<td>12 volts</td>
</tr>
<tr>
<td>7</td>
<td>Modulation Index</td>
<td>0.833</td>
</tr>
<tr>
<td>8</td>
<td>Load inductor</td>
<td>750 µH</td>
</tr>
</tbody>
</table>
Output current of the inverter with specified simulation parameters is shown in Fig. 5.1.

![Output current of the inverter](image1)

Figure 5.1: Simulated output current of 6-Leg inverter at an operating frequency of 5.2 kHz

One of the leg currents with the above mentioned simulation parameters is shown in Fig. 5.2.

![Simulated Leg current](image2)

Figure 5.2: Simulated Leg current of 6-Leg inverter at an operating frequency of 5.2 kHz

Circulating current between two legs is shown in Fig. 5.3. It can be clearly seen that its peak - peak value is below 5% of the maximum output current of 7.07 A.
5.3 Experimental results

Since the inductor is used as load, it draws large currents at low frequencies and low currents at high frequencies. The load inductor used in the experiment is of value 750 \( \mu \)H and it is fabricated using Ferrite core. It has a current rating of 20 A and can be operated from 10 Hz to 20 kHz. The current limit is set to 8 A peak-peak and voltage limit at 20 V peak-peak in the digital controller. The waveforms at operating frequency of 5.2 kHz are obtained with DC bus voltage of 25 V to see the effectiveness of Differential mode filter.

In the voltage mode control, the current will be below the set limit and voltage output of inverter will always be maintained at 20 V peak-peak. This occurs at high frequencies. Whereas in current mode control, the current will be always limited to 8 A peak-peak and voltage will be less than the set limit. The controller initially starts the system in soft start mode and then operates in either voltage mode control or current mode control depending on the load current and load voltage. The soft start modulation signal is shown in Fig. 5.4.

All the voltage waveforms are dominant with switching frequency ripple as no capacitive filter is used in output filter. But this ripple causes no problem during the characterization as the network analyzer extracts only the fundamental component of the waveforms given to the measurement channels. At low operating frequencies the voltage waveform is highly distorted. This is because, the inverter operates at low modulation index to limit the current.
drawn by inductor.

Figure 5.4: Modulation signal from controller during soft start - 2.5 V/div, 1 s/div

The following are the output voltage and current waveforms at different frequencies.

Figure 5.5: CH1(Blue, 50 V/div): Output voltage; CH2(Orange, 1 A/div): Load current; CH3(Green, 2 A/div): Leg A current; CH4(Pink, 2 A/div): Leg B current; MATH CH(Cyan, 1 A/div): Circulating current — $f_m=5.2$ kHz
5.3. Experimental results

Figure 5.6: CH1(Blue, 1 A/div): Load current; CH2(Pink, 10 V/div): Output voltage — $f_m=4.4$ kHz

Figure 5.7: CH1(Blue, 1 A/div): Load current; CH2(Pink, 10 V/div): Output voltage — $f_m=3.0$ kHz
Chapter 5. Simulation and Experimental Results

Figure 5.8: CH1(Blue, 2 A/div): Load current; CH2(Pink, 10 V/div): Output voltage — $f_m=2.0$ kHz

Figure 5.9: CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage — $f_m=1.0$ kHz
5.3. Experimental results

Figure 5.10: CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage — $f_m=880$ Hz

Figure 5.11: CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage — $f_m=725$ Hz
Figure 5.12: CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage — $f_m=625$ Hz

Figure 5.13: CH1(Blue, 5 A/div): Load current; CH2(Pink, 10 V/div): Output voltage — $f_m=500$ Hz
5.3. Experimental results

Figure 5.14: CH1(Blue, 5 A/div): Load current; CH2(Pink, 5 V/div): Output voltage — \( f_m = 200 \) Hz

Figure 5.15: CH1(Blue, 5 A/div): Load current; CH2(Pink, 2.5 V/div): Output voltage — \( f_m = 100 \) Hz
Figure 5.16: CH1(Blue, 5 A/div): Load current; CH2(Pink, 2.5 V/div): Output voltage — \( f_m = 60 \) Hz

Figure 5.17: CH1(Blue, 5 A/div): Load current; CH2(Green, 2 A/div): Leg current; CH3(Pink, 2.5 V/div): Output voltage — \( f_m = 50 \) Hz [CRO in average mode]
5.4 Conclusion

This chapter presented the simulation waveforms of the inverter in open loop operation to validate the different design parameters. The simulation results prove the concept of Differential mode inductor to be effective method of mitigating circulating currents. This is also seen practically in experimental waveforms. Experimental load current and output voltage waveforms of the inverter at different operating frequencies are also presented.

Figure 5.18: CH1(Blue, 5 A/div): Load current; CH2(Green, 2 A/div): Leg current; CH3(Pink, 2.5 V/div): Output voltage — $f_m=29.3$ Hz[CRO in average mode]
Chapter 6

Conclusions

6.1 Summary of the present work

The project was aimed at building the high frequency, high power amplifier for network analyzers to characterize high power devices like transformers, induction machines, synchronous machines etc. A 6-leg single phase inverter topology is used as class - D amplifier to operate at high frequencies with low switching frequency of the switching devices. The topology of the inverter is analysed in detail to design DC bus capacitors, filter inductors and to estimate power loss. Since the switching frequency is high, an analog circuit which can generate triangular carriers of high frequency with required phase shift is also designed. The designed phase shifted carrier board can be used to implement few advanced modulation techniques for both 1-φ and 3-φ Inverters.

Literature survey revealed that not much focus has been made to mitigate circulating currents in single phase inverters connected in parallel. In this project, we have looked at the issue of circulating currents and their mitigation using passive filters. The concept of differential mode inductor is applied to the Multi-Leg single phase inverters with less complexity in their structure to reduce circulating currents. The effectiveness of differential mode inductor has been proven experimentally.

The hardware work involved in the project include —

- Redesigning of Power circuit and its mechanical assembly.
- Design of Phase Shifted Carrier board for sine - triangle modulation of Inverter.
- Soldering and testing of Protection and Delay card, Gate drive cards, Current and Voltage sensing cards etc.
The output current of the Inverter is limited by using a closed loop control strategy, which can work in both current control mode and voltage control mode. This feature allows the load current to be limited by maintaining the maximum possible output voltage. Hence, during characterization of power device we can seamlessly sweep the frequencies of network analyzer without worrying about the load current of Inverter.

Finally, few experiments were carried out by using an inductor as load and results were recorded in both voltage control mode and current control mode. These results validate the concepts discussed. Whereas, at low frequencies we see that the voltage and current waveforms are distorted. This is due to following reasons —

- Forcing the inverter to operate at low modulation index by the control strategy to limit the output current.
- Magnetizing inductance of the differential mode inductors and filter inductors.

### 6.2 Suggestions for future work

1. The issue of distortion in the output voltage due to low modulation index can be resolved. One of the method involves, inclusion of buck converter to regulate the DC bus voltage instead of regulating modulation signals by the implemented control strategy.

2. The circulating currents can be further reduced by using active damping techniques.

3. The switching frequency can be further increased by designing the Gate drive cards using Gate driver IC’s for MOSFETs and by redesigning Protection and Delay cards. This will allow us to operate the Inverter with high modulation frequencies.
Appendix A

Phase Shifted Carrier Generation Board Schematics and its operation details
Appendix A. Phase Shifted Carrier Generation Board Schematics and its operation details
Figure A.1: Phase shifted carrier generator - Channel 1
Figure A.2: PWM pulse generator - Channel 1

Appendix A. Phase Shifted Carrier Generation Board Schematics and its operation details
Figure A.3: Phase shifted carrier generator - Channel 2
Figure A.5: Phase shifted carrier generator - Channel 3
Figure A.6: PWM pulse generator - Channel 3
Figure A.7: Phase shifted carrier generator - Channel 4
Figure A.8: PWM pulse generator - Channel 4
Figure A.9: Phase shifted carrier generator - Channel 5
Appendix A. Phase Shifted Carrier Generation Board Schematics and its operation details

Figure A.10: PWM pulse generator - Channel 5
Figure A.11: Phase shifted carrier generator - Channel 6
Appendix A. Phase Shifted Carrier Generation Board Schematics and its operation details

Figure A.12: PWM pulse generator - Channel 6
Figure A.13: Solder side layout of PSC generation board
Figure A.14: Component side layout of PSC generation board
Figure A.15: Top legend of PSC generation board
Table A.1: Bill of Materials for one channel PSC generation board

<table>
<thead>
<tr>
<th>SI. No.</th>
<th>Part No.</th>
<th>Value</th>
<th>Qty.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U1A, U4A</td>
<td>TL084</td>
<td>2</td>
<td>High slew rate Operational Amplifiers</td>
</tr>
<tr>
<td>2</td>
<td>U5A</td>
<td>LM339</td>
<td>1</td>
<td>Quad Comparator</td>
</tr>
<tr>
<td>3</td>
<td>LD1, LD2</td>
<td>3mm LEDs RED</td>
<td>2</td>
<td>Light Emitting Diodes</td>
</tr>
<tr>
<td>4</td>
<td>R1A, R10A</td>
<td>100KΩ</td>
<td>2</td>
<td>Multiturn potentiometers</td>
</tr>
<tr>
<td>5</td>
<td>R5A</td>
<td>50KΩ</td>
<td>1</td>
<td>Multiturn potentiometer</td>
</tr>
<tr>
<td>6</td>
<td>R2A</td>
<td>1MΩ, 0.25W</td>
<td>1</td>
<td>Carbon film resistor</td>
</tr>
<tr>
<td>7</td>
<td>R3, R11</td>
<td>2.2KΩ, 0.25W</td>
<td>2</td>
<td>Carbon film resistors</td>
</tr>
<tr>
<td>8</td>
<td>R4A, R6A, R7A, R8A, R9A, R35A, R36A</td>
<td>10KΩ, 0.25W</td>
<td>7</td>
<td>Carbon film resistors</td>
</tr>
<tr>
<td>9</td>
<td>R37A, R38A</td>
<td>2.7KΩ, 0.25W</td>
<td>2</td>
<td>Carbon film resistors</td>
</tr>
<tr>
<td>10</td>
<td>C1A</td>
<td>47nf</td>
<td>1</td>
<td>Polycarbonate capacitor</td>
</tr>
<tr>
<td>11</td>
<td>C2A</td>
<td>10nf</td>
<td>1</td>
<td>Polycarbonate capacitor</td>
</tr>
<tr>
<td>12</td>
<td>C3A</td>
<td>4.7nf</td>
<td>1</td>
<td>Polycarbonate capacitor</td>
</tr>
<tr>
<td>13</td>
<td>C4A</td>
<td>1nf</td>
<td>1</td>
<td>Polycarbonate capacitor</td>
</tr>
<tr>
<td>14</td>
<td>C5A</td>
<td>15pf</td>
<td>1</td>
<td>Ceramic disc capacitor</td>
</tr>
<tr>
<td>15</td>
<td>C6A, C7A</td>
<td>10pf</td>
<td>2</td>
<td>Ceramic disc capacitors</td>
</tr>
<tr>
<td>16</td>
<td>C8A, C9A, C17A, C18A, C23A, C24A</td>
<td>0.1µf</td>
<td>6</td>
<td>Ceramic disc capacitors</td>
</tr>
<tr>
<td>17</td>
<td>C15A, C16A</td>
<td>1µf</td>
<td>2</td>
<td>Electrolytic capacitors</td>
</tr>
<tr>
<td>19</td>
<td>TP1A, TP2A, TP3A, TP4A, TP5A, TP6A, TP7A</td>
<td>1 pin bergstrips</td>
<td>7</td>
<td>Test points</td>
</tr>
<tr>
<td>20</td>
<td>J10</td>
<td>3 pin PM connector</td>
<td>1</td>
<td>Power supply point</td>
</tr>
<tr>
<td>21</td>
<td>J9A, J11A</td>
<td>3 pin RM connectors</td>
<td>2</td>
<td>—</td>
</tr>
<tr>
<td>22</td>
<td>J13A, J14A, J15A</td>
<td>2 pin RM connectors</td>
<td>3</td>
<td>—</td>
</tr>
</tbody>
</table>
A.1 Operation details of PSC generation board

Referring to the schematics of PSC generation board follow the steps below —

- Depending on the amplitude of the carrier signals required, choose the capacitors C1, C2, C3, C4, C5, C6 or any combination of them by connecting the jumpers J1, J2, J3, J4, J5 and J6.

- If the modulation signal is same for all the channels, connect the jumpers JP1A, JP1B, JP1C, JP1D and JP1E. Else, remove the jumpers.

- Connect the jumper J8 or J9 depending on whether offset in the carrier is required or not. Do not connect both these jumper together.

- If the offset in the carriers is required, connect the jumper J9 after removing jumper J8 and adjust the potentiometer R10 for offset level adjustment.

- Power the board by connecting the connector J10 to +15 V, 0 V, -15 V power supply.

- Feed the square wave at the connector J14 and using potentiometer R1 adjust the amplitude of carrier when J8 jumper is connected. Potentiometers R5 or R1 can be used to adjust the amplitude of carriers when jumper J9 is connected. Connector J15 can be used to look at the carrier signals in CRO.

- PWM pulse for the top switches of legs in Unit I and Unit II are obtained at connectors J9 and J11 respectively.

- Connectors J9 and J11 are connected to PD card using interleaved interface board to obtain the PWM pulses for bottom switches of inverter with sufficient dead time.
Appendix B

Interleaved Interface Board Schematics
Figure B.1: Interleaved Interface Board
Figure B.2: Solder side layout of Interface Board

Figure B.3: Top legend of Interface Board
Appendix C

Pictures of Hardware
Figure C.1: (1) Phase Shifted Carrier generation board (2) Interface board

Figure C.2: Experimental setup - (1) Unit I of Inverter (2) Unit II of Inverter (3) PSC generation board (4) FPGA digital controller (5) Load Inductor (6) Differential Mode Inductor (7) Filter Inductor
Appendix C. Pictures of Hardware
References


