Analysis, Design and Fabrication Of a Hybrid Series Resonant Converter

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Abstract

A Series Resonant Converter is usually used to generate high voltage power supplies even upto 10kV. These high voltage power supplies which are used in medical and defence applications such as X-Rays etc. A scaled down model of the power converter is to be designed and fabricated at a lower voltage level of 1kV and power level of 250W. The soft switching converter switching frequency was increased to 200kHz inorder to reduce the magnetic components and filter size. The SRC is thoroughly analysed and the results are used to design and fabricate the SRC at the best operating point.

These power supplies frequently encounter pulsed loading in normal operations. A normal closed loop compensated SRC produces ripple at the output voltage due to this. Due to safety considerations, the output capacitor value is limited to store a maximum of 0.5J. Hence an active ripple cancellation technique is suggested to remove the ripple completely using a voltage regulator of lower rating.
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Chapter 1

Introduction

1.1 Introduction to DC to DC Power Converters

With the development of technology, there emerged a huge need to transform DC voltage values so as to suit particular applications. Many electronic circuits were developed following this excessive demand, to transform voltages from certain specific levels (battery voltages available - usually) to that demanded by the load. The early dc-dc converters developed used transistors (usually BJTs) operated in linear mode and were known as Linear Voltage Regulators.

Linear Voltage Regulators used closed loop control to attain the necessary voltage at the output and such that the output voltage is not affected by load changes (Load Regulation). This was achieved by closed loop control which ensures that the remaining voltage appears across the series transistor (controlled element). This configuration was found to be extremely robust to load changes and input voltage changes (within certain limits). These regulators were found to be extremely useful at low power levels. However when the output current (power) is higher, these topologies were found to be inefficient.

The series transistor (controlled element) is operated in linear mode, where it has a considerably large voltage across it (depends on the input supply) and a large current passing through it (depends on the current demanded by the load) at high power levels. There is a huge power loss in the transistor which increases the size of the heat sink and junction temperature. Consequently, the linear regulated power supply becomes inefficient and costly at high power levels. However such converters have very good load and line regulation and zero ripple in the output voltage.

1.2 Introduction to Switched Mode Converters

Further research led to the development of Switched Mode Power Converters (SMPCs), which did not have any drawbacks of the linear voltage regulator. The transistors (usually MOSFETs) were used as switching devices in these converters. The operation of device in switching mode leads to very high efficiency (compared to linear regulators). However, these circuits produce high frequency noise (due to switching), needs complex and large filter circuitry (depending on the power level) and the output contains ripple at switching frequency.
The simple buck converter was one of the first SMPC to be developed. It could transform input voltage to lower levels by appropriate switching of the transistor. An LC filter is used to filter out the high frequency components in the pulsed waveform to obtain near steady dc voltage. However there exists ripple in the output voltage at switching frequency which can be reduced by reducing the cut off frequency of the low pass LC filter at the output. The circuit diagram of the first buck converter is as shown in Figure 1.1.

![Figure 1.1: A Simple Buck Converter Circuit](image)

The boost converter and the buck boost converter helps to attain voltages higher than the input voltage level by appropriate switching actions. These switched mode devices thereby provide higher flexibility to design and greater efficiency compared to the linear mode regulators. Further research led to the development of various topologies of switched mode converters such as Flyback converter, Forward Converter, Half bridge converter etc. These topologies used transformers for stepping up or down the voltage as per requirement in addition to duty ratio control. The usage of transformer facilitated the design of isolated power supply where the output voltage is isolated from the input supply (magnetic isolation) which is required for several applications (medical, gate drive power supply etc).

It can easily be understood that, higher the frequency of operation, lower would be the output ripple voltage. However, the switching losses increase significantly with increase in frequency and thereby reduce the efficiency of the converter and increase the junction temperature. Hence switching frequency emerged as a constraint in design due to switching losses. This led to research into the switching characteristics of various devices under varied load conditions to quantify switching losses. The resistive switching waveforms obtained are as shown in Figure 1.2 (for turn off) and 1.3 (for turn on).

The switching losses can easily be computed from the waveforms for purely resistive load as

\[
E_{off} = \frac{V_{off} \times I_{on} \times t_{on}}{6} \tag{1.1}
\]

\[
E_{on} = \frac{V_{off} \times I_{on} \times t_{off}}{6} \tag{1.2}
\]
However while switching inductive load (which is the usual case where the switching section is followed by a filter), the losses are much more. This can be illustrated using figures which show the waveforms during turn off and turn on as in Figure 1.4 and Figure 1.5 respectively.

The switching loss during inductive turn on and turn off can be calculated as

\[ E_{on} = \frac{V_{off} \times I_{on} \times t_{on}}{2} \]  \hspace{1cm} (1.3)

\[ E_{off} = \frac{V_{off} \times I_{on} \times t_{off}}{2} \]  \hspace{1cm} (1.4)

Hence the total switching power loss for resistive and inductive switching can be calculated as

\[ P_{sw} = (E_{on} + E_{off}) \times f_s \]  \hspace{1cm} (1.5)

It can be seen that for inductive and resistive switching the power loss varies linearly with the frequency of operation. In the case of normal power converter which switches inductive load this increase in the device switching loss with frequency is much more pronounced. Although the use of snubber capacitors can be done to reduce the turn off losses in the device, the turn on losses cannot be readily reduced. Also in the case of RCD snubbers, the turn off losses are removed from the device onto the Resistance (R) in the RCD snubber. Hence the switching frequency cannot be increased above 50kHz for hardswitched converter and cannot be increased above 100kHz for a hard switched converter with snubber protection.
1.3 Introduction to Resonant Power Converters

The resonant power converters use resonant action of LC circuits to artificially introduce soft switching into power converters. The characteristic features of Resonant power converters can be listed as follows.

- Soft switching refers to the switching of the devices under zero voltage or zero current. From the earlier analysis waveforms, we can see that if the converter switches at zero voltage or zero current, then the losses are zero or negligible in a practical case. This facilitates an increase in switching frequency $f_s$ to 100s of kHz without considerable increase in the losses in devices.

- The increase in frequency of operation can help in the reduction of the size of magnetic components and the C filters. This helps in decreasing the overall size of the converter and improving the overall efficiency of the converter.

- Additional inductors and capacitors are necessary to introduce resonant action. Hence additional cost may be incurred in designing these components.

- The VA ratings of the components can increase due to resonant action. The current through the switches can increase due to resonant action and conduction losses may increase.

- Due to ZVS or ZCS action, the EMI issues are very less in resonant converters.

The class of resonant power converters are broadly divided into three categories.

- Load Resonant Converters: In these converters, the load resistance participates in the resonant action and significantly determine the operating point of the converter. The frequency of operation also largely affect the operation and the gain of the converter.

- Quasi-Resonant Converters: In quasi resonant converters, an LC tank is introduced for each switch so that due to resonance the converter can be switched on and off with either zero voltage across it or zero current across it. Unlike load resonant converters which have a fixed topology, the existing converters can be modified to create quasi-resonance and thereby soft switching can be achieved.

- Resonant Transition Converters: Unlike the above two converters, these converters exploits the advantage of zero voltage switching of resonant converters as well as lesser conduction loss of hard switched converters.

The load resonant converters are the most widely used configuration of resonant converters at high frequency switching. These are again classified into different types such as

- Series Resonant Converters: In these converters, the LC tank consists of series connection of the resonant inductor ($L_r$) and resonant capacitor ($C_r$), the load resistance also appears in series with them. Hence the converter can be roughly modelled as a series RLC circuit.

- Parallel Resonant Converters: In parallel resonant converters, the load is connected across or in parallel with the resonant tank capacitor. The transformer output needs an LC filter instead of C filter in series resonant capacitor. Gains greater than one can be obtained using this configuration.
1.4 Objectives of the Project

The main objective of the project is to design a Hybrid Series Resonant Converter which is to be used in X-Ray or radar power supplies. The specifications of the designed converter are as shown in Table.1.1. These power supplies need a high voltage in the range of 1-10kV and has stringent ripple constraints. Moreover in such power supplies, the load is pulsed, ie a short duration of heavy loading is followed by another duration of light loading and this happens at frequencies as high as 5 kHz.

The immediate solution is to design a large enough output capacitor to limit the output voltage ripple within the specified limits. However, a large output filter capacitance stores a large energy. In the case of short circuit, which can happen in X-Ray tubes, even if the converter is switched off fastly by the controller, the energy stored in the output filter capacitor would be dumped into the tube and cause an explosion. Hence due to safety concerns, the output capacitor cannot store energy more than 0.5J.

A linear regulator can be used at the output of the SRC to limit the riplle to very low values. Inorder to use that, a linear regulator needs to be of very high voltage rating. Such a kV or 10kV regulator is extremely costly to design. Hence an active ripple cancellation using a voltage regulator of lower rating is suggested to overcome all these drawbacks. This can be used for effective ripple cancellation.

The design of SRC and active ripple cancellation will be done at a scaled down level of 1kV and ripple cancellation is attempted till 500Hz switching ripple. The objectives of the project can be broken down as points below.

- A thorough analysis and study of the operation of a Series Resonant Converter is to be conducted. The two analysis techniques namely, the sinusoidal approximation technique and normalised technique are to be studied. The analysis techniques are discussed in Chapter1.

- An SRC converter with the following specifications has to be designed and fabricated.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>$V_g$</td>
<td>50 V</td>
</tr>
<tr>
<td>Desired Output Voltage</td>
<td>$V_o$</td>
<td>1kV</td>
</tr>
<tr>
<td>Desired Switching Frequency (Constant)</td>
<td>$F_s$</td>
<td>200kHz</td>
</tr>
<tr>
<td>Maximum Load</td>
<td>$P_{full}$</td>
<td>250W</td>
</tr>
</tbody>
</table>

  Table 1.1: Converter Specifications

The analysis results were used to arrive at the best possible design keeping mind the size, cost and efficiency factors. This is done in the later sections of Chapter 1.

- The hardware design of the high step-up ratio transformer and the resonant components are done in Chapter 3.
The SRC has to be modelled appropriately and a simple controller which assures closed loop stability and maximum possible bandwidth has to be designed. The later sections of Chapter 3 discuss these.

For efficient open loop and closed loop operation of the SRC, certain auxiliary hardware has to be designed such as the voltage sensor, gate driver, load circuit etc. As switching at 200kHz is being attempted for the first time, the gate drivers had to be designed which switch at that high frequency. The load circuit at 1kV/250W needs to be designed such that the load can be switched at frequencies as high as 5kHz. These are done in Chapter 4.

The ZVS ensuring scheme suggested in [1] has to be studied and an attempt has to be made to modify it to improve overall efficiency.

An active ripple cancellation scheme using a lower voltage rated regulator has to be designed to remove the ripple at the output of SRC.
Chapter 2

Series Resonant Converter: Analysis and Design

In this chapter, we discuss the topology of the most suitable power converter to reach the desired specifications, namely the Series Resonant Converter (SRC). The operation of the converter is carefully analysed to find out the resonant tank current which in turn determine the output voltage. The voltage gain of the converter is determined using two different methods which are then compared. The analysis results are studied from the point of view of size, efficiency and economic considerations to arrive at the best steady state operating point of the converter. In the final section, the hardware design for the power converter is proposed.

2.1 Topology of SRC

![Figure 2.1: Topology of SRC](image)
From the figure, an SRC has two inverter legs ($S_1, S_2$ and $S_3$ and $S_4$). Under certain operating conditions, these switches turn on and off softly (either Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS)). The snubber capacitors across each switch ensure ZVS turn off of the switches. These switches are used to apply either a square wave or quasi-square wave across the series resonant section i.e., between $V_1$ and $V_2$ ($V_{inv}$). The resonant components $L_r$ and $C_r$ help the switches attain soft switching as will be explained in later sections.

A high voltage high step-up transformer is necessary to reach the high level of output voltage needed (1kV). A bridge rectifier is used at the output to convert the output voltage to DC. As the converter under optimal conditions are soft switched, the frequency of operation can be increased into 100’s of kHz with comparatively much lesser EMI issues and lossess.

### 2.2 Control Techniques

The three commonly used techniques for controlling the output voltage of an SRC are

#### 2.2.1 Frequency Control

In this method, the frequency at which the inverter leg switches are switched are varied to control the magnitude of the output voltage. An important parameter while discussing the SRC is the Resonant Frequency ($f_r$). Resonant frequency ($f_r$) of SRC is defined as the resonant frequency of the LC tank circuit ($L_r$ and $C_r$).

$$f_r = \frac{1}{2\pi\sqrt{L_rC_r}} \quad (2.1)$$

The system including the resonant tank, output rectifier and the load (modelled as a resistance) can be modelled as an RLC network as shown in Figure2.2. It can be assumed that the inverter legs are used to excite the system with a particular frequency sinusoid. When the excitation frequency or the switching frequency ($F_s$) is lower than the $f_r$, then the impedance offered by $C_r$ is larger than that of $L_r$ and consequently the system behaves as an RC network excited by a sinusoid. Under this condition, the current through the tank will be leading the voltage as shown.

At the switching instant $T_1$ indicated, the switches $S_1$ and $S_4$ (refer to Figure2.1) are turned on and $S_2$ and $S_3$ are turned off simultaneously. At the switching instant $T_1$, the tank current is positive. Hence the switches $S_1$ and $S_4$ turn on with a positive current through it. It can be inferred that for operation below resonant frequency, soft turn on of all the switches cannot be attained. Therefore an SRC is not operated below resonant frequency ($f_r$). The gain when operated in this condition varies from 0 to a maximum of 1 when $f_s$ is almost equal to $f_r$ as can be easily understood from the model.

When the switching frequency is greater than the resonant frequency, the impedance offered by the resonant tank is inductive in nature. Hence the system can be modelled as
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RL circuit for this operating condition as shown in Figure 2.4 where \( L_{\text{eff}} = L_r - \frac{1}{\omega^2 C_r} \).

The tank current would be lagging the applied voltage and will be as shown in Figure 2.5.

As discussed above, at the switching instant \( T_1 \) indicated, the switches \( S_1 \) and \( S_4 \) (refer to Figure 2.1) are turned on and \( S_2 \) and \( S_3 \) are turned off simultaneously. However in this case, at the instant \( T_1 \) the tank current is negative. This means that at \( T_1 \), the current gets transferred from the switch \( S_2 \) to anti-parallel diode of \( S_1 \) and from \( S_3 \) to anti-parallel diode of \( S_4 \). Hence when the switches \( S_1 \) and \( S_4 \) are turned on with zero voltage across them. The presence of snubbers ensure ZVS turn off of \( S_2 \) and \( S_3 \). Hence if \( V_{\text{inv}} \) is a square wave and \( f_s > f_r \), then ZVS can be obtained for all load conditions.

The gain of the normalised power converter model varies from 0 to 1. The maximum gain of 1 is obtained on operation at almost resonant frequency \( (f_s \approx f_r) \) as \( L_{\text{eff}} \) is almost zero then.

In frequency control scheme, the switching frequency is controlled with respect to resonant frequency inorder to control the output voltage. In most of the practical cases, \( f_s \) is greater than \( f_r \) as explained above. Suppose the output voltage is higher than desired, then \( f_s \) is increased such that \( f_s \) moves further away from the resonant frequency. This increases the impedance offered by \( L_{\text{eff}} \) in Figure 2.4, and thereby reducing the output voltage. Similarly inorder to increase the output voltage, \( f_s \) is brought closer to \( f_r \). The exact relationship and deeper understanding is discussed in succeeding sections. The implementation of frequency control using an analog control system is extremely difficult and complicated. They are mostly implemented using microcontrollers, Field Programmable Gate Arrays (FPGAs) etc.
2.2.2 Phase Modulation Control

The two switches of each inverter legs are switched alternately with 50% duty ratio to obtain 0-V\textsubscript{dc} square wave at nodes V\textsubscript{1} and V\textsubscript{2}. The phase difference between these two square waves are controlled so as to control the pulse width of the quasi square wave which gets applied to the resonant section (V\textsubscript{inv}). This pulse width controls the amplitude of the fundamental switching frequency sinusoid which gets applied to the resonant section which in turn determines the output voltage. The technique of using this phase difference between pulses to the two inverter legs to control the output voltage is called Phase Modulation Technique. This is explained in Figure 2.6.

![Figure 2.6: Waveforms explaining Phase Modulation Technique](image)

As explained, in phase modulation method it is the pulse width which controls the output voltage unlike the Frequency control where the pulse width is always one or V\textsubscript{inv} is a square wave. Here the RLC model of the resonant section as in Figure 2.2. can be used for intuitive understanding. As V\textsubscript{inv} is a quasi-square wave, the switching instant does not coincide with the zero crossing of the fundamental of the voltage applied. In frequency control scheme, the switching instant \(T_1\) corresponded to simultaneous turn on of switches S\textsubscript{1} and S\textsubscript{4}. However here, the turn on of one of the switches (say S\textsubscript{1}) happens a certain time (say \(\Delta t\)) before the instant \(T_1\) (this is the zero crossing of the fundamental sinusoid of V\textsubscript{inv}). The turn on of the other switch S\textsubscript{4} happens at \(T_1 + \Delta t\).

As in frequency modulation technique, the power converter is operated usually above resonant frequency \(f_s > f_r\). Hence the current is lagging the fundamental component of V\textsubscript{inv}. However this does not guarantee soft switching as the turn on of S\textsubscript{1} can happen after the zero crossing of current when the current is positive. It can be seen that the switch S\textsubscript{1} on the other leg undergoes soft switching always. A similar analysis shows that switch S\textsubscript{2} always turn on softly while the switch S\textsubscript{3} may not turn on softly. One of the legs which turn on first (ie, before the fundamental zero crossing at \(T_1\)) is termed as the Leading Inverter Leg (here S\textsubscript{1} and S\textsubscript{2}) while the other leg is termed as Lagging Inverter Leg (here S\textsubscript{3} and S\textsubscript{4}). The tank current, V\textsubscript{inv} and fundamental of V\textsubscript{inv} waveforms are as shown in Fig.2.7. when soft switching is happening while the Fig.2.8. shows the waveforms when soft switching is not happening.
2.2.3 Input Voltage Control

In this technique, the converter operates at a constant frequency and constant pulse width of $V_{inv}$ (which can be even 1). The input voltage to the power converter is controlled to attain the desired output voltage level. When the converter is operated in square wave mode of $V_{inv}$ as in frequency control, the converter switches softly for all operating conditions. The drawback is the need of an additional power converter at the input of the same power rating which increases the overall cost of the system and degrades the efficiency.

2.2.4 Mixed Control Scheme

In this method, a combination of frequency control and phase modulation technique is used to control the output voltage. At high loads, pulse width is controlled to maintain a constant output voltage. It can be seen in further sections that at light loads, the pulse widths needed are extremely low and this presents a difficulty in maintaining the output voltage. Hence frequency control can be employed at light loads below a certain threshold.
This helps in controlling in the power converter over a wide load range. However it is extremely difficult to design such a controller in analog domain.

2.3 Analysis of the Converter

In this project, the phase modulation technique (PMT) is used for the control of the power converter (SRC). As discussed the converter need not operate in soft switched mode for entire load range. However the ease of designing a controller in digital domain, ready availability of Phase Modulation Chips such as ML4828 [10] made PMT preferable over other control schemes.

A thorough understanding of the operation of the converter is necessary for efficient design of the power converter. The converter operation can be intuitively understood using the sinusoidal approximation technique as explained in section 2.3.1. In the following section 2.3.2. the converter is analysed accurately through the different time periods to arrive at resonant tank current expression, which in turn is used to compute the gain of the converter.

2.3.1 Sinusoidal Approximation Method

There are certain assumptions used in performing sinusoidal approximation of the Series Resonant Converter. They are

- The bulk of power transfer in the resonant section takes place only through the fundamental of the excitation frequency or switching frequency \( f_s \) or frequency of the quasi square wave. A correction factor is incorporated to account for the harmonic power transfer.

- The output voltage is assumed to be a constant and it is reflected into the primary as a square wave.

- This square wave is assumed to be in phase with the fundamental of the tank current waveform. Plainly, the amount of harmonics in the resonant tank current is negligible.

![Figure 2.9: Model for Sinusoidal Approximation of SRC](image-url)

\[
\frac{\omega L_r j}{\omega C_r j} \frac{V_g}{I_r} = \frac{V_o^2}{R^*}
\]
The normalised model of the power converter for sinusoidal approximation is as shown in Figure 2.9. In the process of normalisation, the effect of transformer is accounted for. \( R^* \) represents the normalised load resistance resistance appearing on the primary), \( V_o \) is the normalised output dc voltage.

\[
V_o = \frac{2 \times I_r \times R^*}{\pi} \tag{2.2}
\]

\( V_{o2} \) represents the fundamental of the reflected square wave on the primary. As mentioned in the assumptions, we neglect the harmonics. \( V_{o2} \) can be derived as

\[
V_{o2} = \frac{4 \times V_o}{\pi} \tag{2.3}
\]

The impedance offered by resonant capacitor(\( C_r \)) and the resonant inductor (\( L_r \)) can be modelled as single impedance (\( Z_{ef} \)). This impedance will be inductive in nature due to above resonant operation. The phasor diagram obtained from the model can be drawn as shown in Figure 2.10.

\[
Z_{ef} = \frac{2\pi f_s \times (L_r - \frac{1}{C_r})}{j} \tag{2.4}
\]

![Figure 2.10: Phasor Diagram for Sinusoidal Approximation Model](image)

![Figure 2.11: Harmonic Model](image)

From the phasor diagram, we can write

\[
\vec{V}_g = \vec{V}_o + I_r \vec{Z}_r \tag{2.5}
\]

Solving this vector equation using previous equations 2.2,2.3 and 2.4, the final expression for gain can be obtained as

\[
G(\frac{V_o}{V_{in}}) = \frac{8R \times sin(\frac{\pi D}{2})}{\pi^2} \times \frac{1}{\sqrt{\left(\frac{(f_s/f_r)^2-1}{2\pi f_s C_r}\right)^2 + \frac{64 \times R^2}{\pi^4}}} \tag{2.6}
\]
Here $f_r$ represents the resonant frequency and $D$ represents the pulse width or the duty ratio of the quasi square wave $V_{inv}$. It can be seen clearly from the expression that the gain of the converter depends on

- The switching frequency ($f_s$).
- The resonant frequency ($f_r$).
- The surge impedance of the resonant tank ($Z_r = \sqrt{L_r/C_r}$). Instead of characterising the resonant tank as $L_r$ and $C_r$, it is simpler to characterise the tank as $f_r$ and $Z_r$.
- The load resistance.
- The pulse width or the duty ratio of the quasi square wave ($V_{inv}$).

However, we can see in the later section that these absolute values are not determining the gain, but the relative value of $f_s$ with respect to $f_r$, relative value of $R$ with respect to $Z_r$. The power transferred at harmonic frequencies were also computed and incorporated as a correction factor to obtain the final gain. The graphical results of this analysis are available in section 2.3.3.

### 2.3.2 A Normalised Accurate Analysis

A normalised approach was used to find out the accurate tank current waveform by using exact differential equations for each sub-period. The assumptions used in this method are

- The switches and the resonant tank components are considered ideal and they offer no resistance.
- The transformer is ideal and has zero parasitic capacitance. Hence the waveform appearing across the primary is a square wave whose zero crossing is same as the zero crossing of the tank current.
- All the filter components are ideal and load is purely resistive.

If we consider each sub-interval, we can see that the resonant tank is excited by two sources. The inverter legs switch to excite the tank with a quasi square wave (dc at a particular instant) and the transformer excites it with a square wave which is dependent on the current (dc at a particular instant) as shown in Figure 2.12. We can divide these into a certain number of sub-intervals where the tank is excited by a simple dc source and the tank having certain initial conditions as shown in Figure 2.13.

For each sub-interval, when the resonant section is excited by a DC source, the generalised differential equation for the resonant section can be derived from the Figure 2.13. as

$$V_s = L_r \frac{dI_r}{dt} + V_c$$  \hspace{1cm} (2.7)
We need to note that the initial conditions are different for each sub-intervals. The inductor current ($I_r$) and the capacitor voltage ($V_c$) at the end of a sub-interval $T_1$ serves as the initial condition for the sub-interval $T_2$. In steady-state, the final condition of the last sub-interval serves as the initial condition for the first sub-interval. Also due to half-wave symmetry of the excitation waveforms and linearity of the resonant section, we need to analyse only for a half wave to arrive at expressions for current. The above differential equations can be solved for a general initial condition with ($I_o$) and ($V_{co}$) as initial inductor current and capacitor voltage respectively as shown.

$$I_r(t) = I_o \cos(w_r t) + \frac{V_s - V_{co}}{Z_c} \sin(w_r t)$$

$$V_c(t) = V_s + (V_s - V_{co}) \cos(w_r t) + Z_c I_o \sin(w_r t)$$

The analysis of the converter using these equations over the entire sub-cycles is extremely complicated. Hence a normalisation technique is used as in [1]. This simplifies analysis to a considerable extent. The bases chosen are as in Table 2.1.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Base Chosen</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Base</td>
<td>Input Voltage to Power Converter</td>
<td>$V_g$</td>
</tr>
<tr>
<td>Impedance Base</td>
<td>Surge Impedance of LC tank</td>
<td>$Z_r = \sqrt{\frac{L_r}{C_r}}$</td>
</tr>
<tr>
<td>Current Base</td>
<td>$I_B$</td>
<td>$I_B = \frac{V_g}{Z_c}$</td>
</tr>
<tr>
<td>Frequency Base</td>
<td>Resonant Frequency</td>
<td>$f_r = \sqrt{\frac{1}{4\pi^2 L_r C_r}}$</td>
</tr>
</tbody>
</table>

Table 2.1: Bases for Normalised Analysis

It is observed that the converter operates in three distinct modes [1]. From our initial RLC model analysis using quasi square wave excitation, we observed that there exist one
mode where the switching of lagging leg (S4) happens when the current is still negative and lagging leg undergoes ZVS turn on. This mode is termed as Mode 1 throughout the report.

There exists two visibly distinct modes when the current reaches zero before the lagging leg turn on. In one of the modes, termed Mode2 hereafter, the current reaches zero and becomes positive before lagging leg turn on. This can happen only if the normalised capacitor voltage when the current reaches zero (Vc0) is greater than the normalised output voltage to turn on the rectifier diodes. Otherwise the diodes remain off and the Ir remains zero till the lagging leg turns on. This mode of operation is termed as Mode3 hereafter. In Mode3, the lagging leg switches undergo ZCS turn on as the current remains at zero at the time of turn on.

Consider Mode1 operation, a half-wave sub-interval is as shown in Figure 2.14. During the interval I1, the current is negative but Vinv is zero. Hence it Vo (normalised output voltage) is driving the tank system as shown in Figure 2.15. This can be substituted into equations 2.9 and 2.10 to derive the expression for sub-interval I1.

\[
\text{Figure 2.14: Waveforms for Explaining Mode 1 Operation}
\]

\[
\text{Figure 2.15: Sub-Interval I1}
\]

\[
\text{Figure 2.16: Sub-Interval I2}
\]

\[
\text{Figure 2.17: Sub-Interval I3}
\]

It can be seen that during the sub-interval I1, power is being freewheeled ie, the resonant section is providing power to the load. In the sub-interval I2, the voltage is positive and the current is negative, hence here the current is being fed back into the source. It is only during the sub-interval I3 (during the positive half cycle) that the power is being supplied by the source to the resonant section and the load. Hence if A1, A2, A3 are the areas under the current waveforms in respective time periods, then using power balance in normalised domain gives
\[ M \times (A_1 + A_2 + A_3) = 1 \times (A_3 - A_2) \Rightarrow M = \frac{A_3 - A_2}{A_1 + A_2 + A_3} \]  
(2.11)

By using the normalised general expression and the excitation voltage from the sub-interval modes coupled with the fact that the initial condition for current in sub-interval I1 is the negative of the final condition of current in sub-interval I3 can be used to solve for the normalised gain of the converter (M) and the time period \( t_v = T_2 - T_1 \). The duration of sub-interval I1 depends on the pulse width while the duration of sub-interval I2 \( t_v \) depends on the parameters of the circuit while duration of sub-interval I3 is \( T_2 - T_2 \) (this again depends on the circuit parameters.

For simplified analysis, certain terms have to be defined such as Q factor of the circuit \( Q \), frequency factor of operation \( f_r \).

\[ Q \text{Factor}(Q) = \frac{Z_r}{R} = \sqrt{\frac{L_r}{C_r}} \]  
(2.12)

\[ Frequency \text{Factor}(f_r) = \frac{f_s}{f_r} \]  
(2.13)

\[ \theta_v = 2 \times \pi \times t_v \times f_r \]  
(2.14)

The entire Mode 1 operation finally breaks down into two equations as shown.

\[ M_{num} = (1 - M + \frac{MQ\gamma}{2}) \times (1 - \cos((D\gamma) - \theta_v)) + (1 + M + \frac{MQ\gamma}{2}) \times (\cos(\theta_v) - 1) \]  
(2.15)

\[ M_{den} = (1 - M + \frac{MQ\gamma}{2}) \times (1 - \cos((D\gamma) - \theta_v)) - (1 + M + \frac{MQ\gamma}{2}) \times (\cos(\theta_v) - 1) \]  

\[ + (1 - M + \frac{MQ\gamma}{2}) \times (\cos(\gamma - \theta_v) - \cos(\gamma - \theta_v)) + \cos(\gamma - D\gamma) - 1 \]  
(2.16)

\[ M = \frac{M_{num}}{M_{den}} \]  
(2.17)

\[ \theta_v = \tan^{-1} \left( \frac{(1 - M + \frac{MQ\gamma}{2}) \times (\sin\gamma)}{(1 + M + \frac{MQ\gamma}{2}) + ((1 - M + \frac{MQ\gamma}{2}) \times \sin\gamma)} \right) \]  
(2.18)

The above 4 equations were solved using Newton Raphson Method in MATLAB and the results will be presented in the next section. A detailed expansion of the method and equations arrived at is available in [1]. A corrected form of the equations in [1], clearing it of minor errors is presented above. The MATLAB code is presented in Appendix.A.

In a similar way, the Mode 2 and Mode 3 can be analysed. The tank current and \( V_{inv} \) waveforms are presented including the various sub-intervals for Mode2 and Mode3 in Figures 2.18. and 2.19. respectively.

In Mode2 operation, it can be seen that the current reduces to zero before the switching on of \( S_4 \) happens and it continues to increase in the positive direction. The lagging leg
switches have hard turn on in this mode of operation. This happens as the capacitor voltage when the current is zero \( V_{cio} \) is greater than the normalised output voltage and thereby turns on the other set of diode for reverse direction. The analysis result shows that the normalised peak capacitor voltage \( V_{cpeak} \) corresponds to the current zero condition and its magnitude is obtained as

\[
V_{cpeak} = \frac{MQ\gamma}{2}
\]  
(2.19)

For the current to increase in the other direction before turn on of lagging leg

\[
V_{cpeak} > M \Rightarrow Q > 2\gamma
\]  
(2.20)

Hence \( Q=2/\gamma \) is the boundary condition for Mode2 and Mode3 as long as the current reaches zero before lagging leg turn on. The sub-interval I4 is unique to Mode2 operation. The expressions derived for Mode3 operation is presented in Appendix.A.

In Mode3 operation, the current remains at zero once it becomes zero till the lagging leg switch is turned on. This provides a ZCS turn on for the lagging leg switches. The resonant capacitor voltage \( V_c \) is clamped at its peak value in the sub-interval I5 when the current remains zero. In a similar way, the analysis for Mode3 operation was carried out and expressions are available in Appendix.A.

The MATLAB code presented in Appendix.B. solves the normalised SRC for specified inputs such as frequency factor, Q factor, pulse width etc. This was used to study the converter performance over a wide range of input variables.

2.3.3 Analysis Results and Comparison of the Two Methods

Intuitively we can say that as the pulse width of the quasi square wave is increased, the fundamental switching frequency component in \( V_{inv} \) also increases and hence the output voltage should also increase. Figure 2.20. shows the variation of the Normalised gain M with the pulse width \( D \) at a particular Q factor and frequency factor of 4.0 and 1.15 respectively.

It can be seen from Figure 2.20. that at very high duty ratios the sinusoidal approximation has significant error. It also shows that the practical gain would be significantly less (by 4%) at high duty ratios compared to the approximate analysis. Figure 2.21.
Figure 2.20: Gain vs Pulse Width for the two methods

shows the variation of the gain of the converter over a range of Q factors keeping pulse width constant at 0.8 and frequency factor constant at 1.15.

Figure 2.21: Gain vs Q factor for the two methods

From the figure, we can see that at higher Q factors the approximate method approaches the accurate result. The error is considerably less at high Q factors. At high Q factors, the effect of resistance and the rectifier part is lesser compared to the resonant tank part. The resonant tank which is linear is more dominant in determining the tank current waveform. The tank also offers higher impedance at higher harmonics present in the excitation voltage. Due to all these, the current is closer to a sinusoidal at higher Q factors. At lower Q factors, the resistive part is more dominant, the converter moves to hard switching Mode2 or Mode3 and current contains higher quantity of high frequency harmonics and therefore larger error.

As the frequency factor is increased, we can see that the impedance offered by the resonant tank increases. If the Q factor and pulse width of the quasi-square wave
are kept constant, then the gain of the converter decreases with an increase in frequency factor. Actual quantisation of the gain can be obtained using either of the two methods. Figure 2.22. shows the variation of the gain with frequency factor for constant Q factor of 4.0 and constant pulse width of 0.95. At high frequency factors, the resonant tank section is more dominating and the waveform contains less harmonics and approximate solution approaches the normalised accurate solutions.

2.4 Design Considerations for the SRC

From the analysis results, it is clear that the gain of a normalised ideal Series Resonant Converter depends on these three factors.

• The Pulse Width of applied quasi-square wave ($V_{inv}$). The converter gain increases with an increase in pulse width as shown in Figure 2.20.

• The frequency factor ($f_f$). The converter gain decreases with an increase in frequency factor as shown in Figure 2.22.

• The Q factor of the circuit ($Q$). The converter gain decreases with an increase in Q factor as shown in Figure 2.21.

The design of practical converter requires consideration of several other factors not only the gain. In order to achieve the mentioned specification of converting 50V to 1kV, a step up transformer is necessary. The voltage and current rating of the Resonant Tank should also be minimised for designing a cost efficient system. As observed earlier, the converter when operated in phase controlled mode need not always operate in soft switching mode. The converter should also be designed such that it operates in soft switching range for a region as large as possible. These are the points kept in mind while designing the converter.

As observed as the frequency factor is increased, the impedance offered by the resonant tank increases and the output gain decreases. Hence a higher turns ratio transformer
is required to achieve the specified gain. This variation of transformer turns ratio (N) needed with respect to frequency factor ($f_f$) is shown in Figure 2.23 at constant Q factor of 4.0 and Pulse width of 0.8. Similarly an increase in Q factor symbolises a decrease in the load resistance when $f_f$ is fixed and the impedance offered by the tank remains constant. This leads to decrease in gain and consequently a higher turns ratio transformer is needed to attain specified voltage. This variation of turns ratio (N) vs Q is shown in Figure 2.24 at $f_f = 1.15$ and D=0.8.

The increase in frequency factor, increases the impedance offered by the tank. Hence if we consider the simplified RLC model for intuitive understanding, we can see that while the load resistance remains constant, increase in tank impedance causes an overall increase in the RLC section and thereby reducing the current. The exact variation is as shown in Figure 2.25, which shows the variation of RMS Current Rating with $f_f$ at Q=4.0 and D=0.8. While increasing the Q factor, reduces the load resistance and the effective impedance of the RLC path decreases and the tank current rating increases. This variation of tank Current Rating and Tank capacitor voltage rating with Q factor at $f_f = 1.15$ and D=0.8 is shown in Figure 2.26 and 2.28, respectively.

Figure 2.29 shows the variation of Modes of operation of the converter with frequency factor ($f_f$). From the RLC model discussed earlier we can see that at low $f_f$ the resistance
is the dominating factor in the impedance. Hence the phase lag of the tank current is lesser and the converter operates in Mode1 for a smaller range. The range of Mode3 increases marginally with $f_f$ according to the formula ($Q_{bound} = \frac{2}{\gamma}$). As the frequency factor is increased, the phase lag of current increases and thereby the range of Mode1 increases. This is observed in the Figure 2.29. Similarly if we are decreasing the maximum Q factor of operation, the resistive part in RLC model is becoming more dominant. Hence the range of Mode1 operation decreases as we decrease the maximum Q factor of operation. This is observed in Figure 2.30.

### 2.5 Design: Operating Point Selection

The analysis results were thoroughly studied to choose the operating point which

- Minimised Turns Ratio of the Transformer.
- Minimal Current and Voltage Ratings of the Tank Components.
- Maximum region of Mode1 or Mode3 Operation.
Although from the point of view of the current ratings and the % region of ZVS operation, a high frequency factor of operation appears attractive and advantageous, these operating conditions have very low gain and consequently a very high turns ratio transformer is needed. There are several constraints in increasing the turns ratio of transformer above 1:40. The parasitics of the transformer becomes very high and affects the operation of the circuit and such a high turns ratio transformer is not cost efficient. Hence high frequency factor is not preferred for the design.

At low frequency factors, although the transformer turns ratio becomes less (even less than 30), the current ratings are very high and the region of ZVS operation is very low under these operating conditions. The main advantage of SRC was the possibility of exploiting soft switching which is not available in this operating condition. Hence a moderate value of frequency factor of 1.15 was chosen for the design of the converter.

At high Q factors, the current and voltage ratings of the resonant components are very high and the gain of the converter is extremely low although it may have large range of Mode1 operation. While at low Q factors, there is very less chance of exploiting the advantages of soft switching. Hence a moderately high Q factor of 4.0 was chosen for operation.

The maximum duty ratio of operation was selected as 0.8 (D) which corresponded to a normalised gain 0.543 at maximum Q factor. This needed a transformer of turns ratio 1:38 which can be practically fabricated within the parasitic limits.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Factor</td>
<td>( f_f )</td>
<td>1.15</td>
</tr>
<tr>
<td>Maximum Q factor</td>
<td>( Q )</td>
<td>4.00</td>
</tr>
<tr>
<td>Turns Ratio of the Transformer</td>
<td>( N )</td>
<td>1:38</td>
</tr>
<tr>
<td>Voltage rating of the capacitor</td>
<td>( V_c )</td>
<td>105V</td>
</tr>
<tr>
<td>Current Rating of the Tank</td>
<td>( I_r )</td>
<td>10.8A</td>
</tr>
</tbody>
</table>

Table 2.2: Operating Conditions

From the specifications, the maximum load on the converter is 250W which corresponds to the maximum Q factor of 4.00. At 1kV output voltage, maximum load resistance corresponds to 4kΩ. At zero load (not a practical situation), even a small pulse width can cause a normalised gain of 1 and an output voltage of \( 38 \times V_g = 1900 \text{V} \). Hence the converter is uncontrollable at zero load. However in a practical case, there is some minimum load on the converter due to ESR of filter capacitor, losses in switches etc. However for the control and design aspects, a minimum load of 20W is considered.

From Figure 2.31, it can be seen that the converting operates in Mode1 from 65% load to the full load while operating at the specified operating conditions harnessing the
advantages of ZVS turn on. Under this condition, the leading leg and the lagging leg turns on and off in a ZVS way. From no load to 20% load, the converter operates in Mode3 where the lagging leg turns on in a ZCS way while all other switchings are happening softly. From 20% to 65% load, the converter operates in Mode2, where the lagging leg ($S_3$ and $S_4$) turns on in a hard way while all other switchings happen in a soft way. A method of using an auxiliary inductor to attain ZVS turn on of lagging leg switches under any operating condition is studied in a later chapter [1]. A method of increasing the efficiency of this method is suggested.
Chapter 3

Hardware and Controller Design

The initial section of this chapter discusses the challenges involved and the solutions for designing and fabricating the hardware for the theoretically designed converter. The converter was fabricated on a Printed Circuit Board (PCB) : IISc/Sandeep Warrier Resonant Converter PCB V1.0. The subsequent section discusses an appropriate modelling technique for the converter. Due to high degrees of non-linearity and the resultant complexity involved in using Averaged Modelling for this converter, an approximate model is arrived at based on the responses of the system. The design of a stable and considerably fast controller is made using the converter model. The subsequent section discusses the implementation of the controller on an FPGA platform. The design of auxiliary hardware for closed loop action of the converter is discussed later. The last section presents the experimental results.

3.1 Hardware Design of the SRC

Due to the development of high speed switching devices, a switching frequency $f_s$ of 200kHz is chosen for the Series Resonant Converter. An increased switching frequency helps in the reduction of the size of the Resonant Tank components which in turn reduces the losses in these components and improves the overall efficiency. From the chosen frequency factor, the resonant frequency of the resonant tank can be found out as

$$f_r = \frac{f_s}{1.15} = 173.913kHz$$  \hspace{1cm} (3.1)

The load resistance under full load condition for 250W is 4kΩ. Hence the equivalent resistance referred to the primary side can be computed as

$$R_e = \frac{R_L}{N^2} = \frac{4000}{38^2} = 2.77\Omega$$  \hspace{1cm} (3.2)

The surge impedance ($Z_r$) can be computed from the equivalent resistance and Q factor as

$$Q = \frac{Z_r}{R_e} \Rightarrow Z_r = R_e \times Q = 11.0803$$  \hspace{1cm} (3.3)

The value of $f_r$ along with $Z_r$ can be used to find out the resonant capacitor and inductor ($L_r$ and $C_r$) values as
\[ L_r = \frac{Z_r}{2\pi f_r} = 10.14 \mu H \]  

(3.4)

\[ C_r = \frac{L_r}{Z_r^2} = \frac{10.14 \mu}{11.083^2} = 82.54 nF \]  

(3.5)

### 3.1.1 Switches and Gate Drive Design

The RMS tank current was found to be 10.8 A. The peak tank current is necessary for proper design of the magnetic components- inductor \(L_r\) and transformer. The switches should block the dc bus voltage when they are off, as the complementary switch would be conducting. Hence the factors that influence switch selection are

- Peak current through the switch at full load = 16A
- Peak blocking voltage for the switch = \(V_g = 50V\)
- Ability to be switched at the very high frequency of 200kHz.
- Must be capable of being turned on by 15V.

Based on the above considerations, IRF540 [11] was selected as switches for both the legs. It has very low resistance \(R_{on}\) of 44\(m\Omega\) and hence doesnot alter the operating point of the converter.

For the complementary switching of an inverter leg, IRS2110 was used. It creates an isolated voltage of 15V (voltage supplied as its input-\(V_{cc}\)) using bootstrap action. From the datasheet of IRS2110 [12] the design equations for the bootstrap capacitor and diodes are obtained. The bootstrap action can be explained using Figure.3.1.

![Figure 3.1: Gate Driver block diagram](image)

The bottom switch \(S_2\) is driven by a complementary signal to the top switch. Hence when \(S_2\) is on, the bootstrap capacitor \(C_b\) gets charged through the bootstrap diode to \(V_{cc}\). Once the switch \(S_2\) is turned off just prior to the turn on of \(S_1\), the bootstrap diode is turned off and thereby a temporary isolated voltage \(V_{cc}\) is available for driving the gate of \(S_1\). The criterion for designing the bootstrap capacitance is that the voltage across the capacitance doesnot get reduced by more than 0.5V as it drives the gate of top switch \(S_1\). Hence the charge stored in the capacitance should be high enough to supply the gate charge for turn on and various other leakage factors. Based on these considerations and...
using the application note of IRS2110 [13], the bootstrap capacitance \( C_b \) was selected as 2.2\( \mu \)H. The bootstrap diode was selected such that it can be operated at fast frequency of 200kHz and it blocks a reverse voltage of atleast \( V_{dc} + V_{cc} \) where \( V_{dc} \) is the dc bus voltage. The total losses in the driver circuitry was estimated to be 0.4W when operated at 200kHz.

For negative conduction during the positive half cycle when the leading leg switch \( S_1 \) is on, the anti-parallel diode inbuilt in the MOSFET IRF540 is used. The relative periods of conduction for the anti-parallel diodes of \( S_1 \) and \( S_2 \) are the same. Hence the leading leg switches \( S_1 \) and \( S_2 \) have the same conduction losses. However when we compare the leading leg to the lagging leg, we can see that the periods of conduction for anti-parallel diodes are not equal. The leading legs have larger periods of anti-parallel diode conduction than the lagging leg switches. This results in a slight difference in the conduction losses of both the legs and results in slight asymmetry in heating.

![Figure 3.2: Waveforms for explaining Conduction Loss of Switches](image)

From the Figure.3.2., during the sub-intervals I2 and I3 the performance of the leading leg and lagging leg switches are identical. Hence they produce similar losses in those sub-intervals. However, the difference between \( S_1 \) and \( S_4 \) lies in the sub-intervals I1 and I1*. The current waveforms are similar during sub-intervals I1 and I1*, however they are of opposite polarity. Hence in sub-interval I1, it is the anti-parallel diode of \( S_1 \) which is conducting and in interval I1* it is the switch \( S_4 \) which is conducting. Therefore, the conduction losses can be found out as

\[
P_{\text{leadloss}} = \int_{T_0}^{T_1} V_d \times i_r \times dt + \int_{T_1}^{T_2} V_d \times i_r \times dt + \int_{T_2}^{T_3} i_r^2 \times dt = 3.802W. \quad (3.6)
\]

\[
P_{\text{lagloss}} = \int_{T_2}^{T_3} V_d \times i_r \times dt + \int_{T_3}^{T_4} i_r^2 \times dt + \int_{T_4}^{T_1*} i_r^2 \times dt = 3.209W. \quad (3.7)
\]

where \( P_{\text{leadloss}} \) and \( P_{\text{lagloss}} \) represents the maximum conduction loss of the leading and lagging leg respectively. The turn on losses are negligible when the switches turn on softly. However, the use of snubbers does not remove the turn off losses entirely. These depend on the value of snubber capacitance and hence will be calculated in a later section after the design of snubber capacitor. These can be expected to be very low (say < 1W).
3.1.2 Step-Up Transformer Design

The design of the Step-Up transformer is the most critical part in the design of the SRC. The following are the important points which are to be considered while designing the transformer for the designed SRC converter.

- The turns ratio to be attained is $N_p : N_s = 1 : 38$.
- The parasitic capacitance ($C_p$) of the transformer referred to the primary appears in the resonant path and can influence the response of the SRC. This should be less than the resonant capacitor $C_r$ by at least ten times.
- The magnetising inductance of the transformer ($L_m$) should at least be 4 times greater than the resonant inductor $L_r$ so that it does not influence the response of the SRC.
- The transformer is a square wave transformer with a VA rating of 285VA.
- The frequency of operation is 200kHz. This affects the size of the core of the transformer and the choice of conductors so as to reduce the skin effect.
- The RMS primary current rating is 10.8A. This affects the size of the conductors.

The design was finalised using a combination of the conventional transformer design method mentioned in [2] along with a trial and error method as $L_m$ and $C_p$ are extremely crucial to the design.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Equation</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core used</td>
<td></td>
<td>ETD59</td>
</tr>
<tr>
<td>Number of turns of Primary</td>
<td>$N_p$</td>
<td>3</td>
</tr>
<tr>
<td>Number of turns of secondary</td>
<td>$N_s$</td>
<td>114</td>
</tr>
<tr>
<td>Maximum flux density</td>
<td>$\frac{V_p}{4JNA_c}$</td>
<td>0.02T</td>
</tr>
<tr>
<td>Magnetising inductance</td>
<td>$L_m = \frac{N_p^2}{8f}$</td>
<td>80.66$\mu$H</td>
</tr>
<tr>
<td>Leakage Inductance</td>
<td>$L_l$</td>
<td>2$\mu$H</td>
</tr>
<tr>
<td>Winding factor</td>
<td>$K_w = \frac{A_w}{N_p A_{pw} + N_s A_{sw}}$</td>
<td>0.0628</td>
</tr>
<tr>
<td>Parasitic Capacitance(layer to layer)</td>
<td>$C_{pll}$</td>
<td>1.2nF</td>
</tr>
<tr>
<td>Core Loss</td>
<td>$P_{core}$</td>
<td>1.45W</td>
</tr>
<tr>
<td>Copper Loss</td>
<td>$P_{cua}$</td>
<td>0.47W</td>
</tr>
</tbody>
</table>

Table 3.1: Table of Transformer Parameters
The chosen design is the best trade off between all the mentioned factors. The reduced $B_m$ ensures that the core loss of the transformer is lower. The primary current through the transformer has a maximum rms value of 10.8A and is at 200kHz frequency. This can cause a huge increase in copper loss if a single strand wire is used. The cross sectional area of the primary winding needed was computed as

$$A_{pw} = \frac{10.8}{2.5A/mm^2} = 4.32mm^2$$  \hspace{1cm} (3.8)

The skin depth of the copper wire at this frequency of 200kHz was calculated as

$$\text{Skindepth}(\rho) = \frac{1}{\omega \times \epsilon \times \mu} = 0.1mm.$$  \hspace{1cm} (3.9)

In order to reduce the increase in resistance due to skin effect at high frequency, the primary was made of 68 strands of SWG30 in parallel, in 4 groups of 17 in each (litz wire). This reduces the copper losses in transformer considerably. Similarly, the secondary was wound with 3 wires of SWG 32 stranded together to form litz wire.

The frequency response of the practically wound transformer was obtained using the network analyser as shown in Figure 3.3. It can be observed that the resonant frequency ($F_{tres}$) is 1.5MHz for the transformer.

$$F_{tres} = \frac{1}{2\pi \sqrt{(L_p || L_m)C_p}}$$  \hspace{1cm} (3.11)

Hence the measured parasitic capacitance was $C_p = 4.8nF$ which was well less than one tenth of the resonant capacitor.
3.1.3 Design of the Resonant Inductor

The design of the resonant inductor is an integral part of the design of a Series Resonant Converter. The points which are considered while designing the Resonant Inductor $L_r$ are as follows

- The RMS current through the tank which determines the cross-sectional area of the wire used for winding the inductor.
- The peak tank current, to ensure that even at that current the core of the inductor does not get saturated.
- The frequency operation affects the choice of the conductors so as to minimise the skin effect.
- The leakage inductance of the transformer referred to the primary($L_{lp}$) appears in series with the resonant inductor. Hence the designed value of resonant inductor should be

$$L_{rprac} = L_r - L_{lp} = 10.24\mu H - 4.7\mu H = 5.54\mu H.$$  \hspace{1cm} (3.12)

The area product was computed as

$$A_c \times A_w = \frac{L \times I_{lp} \times I_{rms}}{B_{max} \times J \times K_w} = 13440 mm^2$$  \hspace{1cm} (3.13)

where $K_w$ was the winding factor. The core chosen was slightly larger than the computed area product so as to have flexibility in reduction of core loss. E42/21/15 was selected.

As the current through the resonant tank inductor is same as the primary current through the transformer, a similar configuration of conductors are used as in the step-up transformer. The conductors consist of 68 strands of SWG32 in parallel which are stranded together into 4 groups of 17 in each similar to litz wire. This reduces the copper losses in the inductor. The number of turns were found out such that the core does not saturate even under peak current condition.

$$N \geq \frac{L_{rprac} \times I_{peak}}{B_{max} \times A_c} \implies N \geq 3$$  \hspace{1cm} (3.14)

In order to reduce the core loss by reducing the $B_m$(maximum flux density of operation), number of turns were chosen as $N=5$. Hence $B_m$ was reduced to 0.121T and thereby reducing the Core loss in resonant inductor to 11W. The airgap length needed was calculated as

$$l_g = \frac{\mu_o \times N \times I_{peak}}{B_m} = 0.83 mm.$$  \hspace{1cm} (3.15)

The winding factor was calculated as

$$K_w = \frac{N \times a_w}{A_w} = 0.08$$  \hspace{1cm} (3.16)

The total resistance offered by the winding was calculated as
\[ R_L = \frac{l_w \times 291\Omega/km \times 10^{-6}}{68} = 1.372m\Omega \]  

(3.17)

where \( l_w \) is the length of one strand of SWG 32 wire. The copper loss was calculated as 0.2W.

### 3.1.4 Design of Resonant Capacitor

The following points are considered while selecting the resonant capacitor.

- The capacitor should be capable of operation at very high frequency of 200kHz ie, the self resonant frequency of capacitor should be as far away from 200kHz as possible. Hence ceramic or mica capacitors are preferred.
- The RMS current rating of the capacitor should be greater than 11A. This cannot be achieved using a single ceramic capacitor. Mica capacitors have higher current ratings in range of 5A, but are not cost efficient.
- Voltage rating should be greater than 105V.
- \( C_r = 82.54nF \).

Based on the above considerations, a parallel combination of 18 similar capacitors of 4.7nF were used. SMD ceramic capacitors were used to save space and they have very high self-resonant frequency (VJ 1812Y472KXEAT5Z (4.7nF))[15]. These capacitors have very low ESR of 0.119m\( \Omega \). Hence the losses are negligible.

### 3.1.5 Design of Rectifier and Output Filter

The RMS current through the diodes on the secondary side

\[ I_{drms} = \frac{10.8}{N} = \frac{10.8}{38} = 0.284A \]  

(3.18)

They should operate at high frequency of 200kHz and should block a peak inverse voltage of atleast 1kV. Hence 8 diodes of MUR1100 are used to form the diode bridge rectifier section as shown in Figure.3.5.

![Rectifier Schematic](image)

Figure 3.5: Rectifier Schematic

![Filter Current Waveform](image)

Figure 3.6: Filter Current Waveform
The output filter is designed such that under full load the maximum output voltage ripple is 1%. The tank current is assumed sinusoidal for the analysis. It is assumed that the entire ripple in the rectified sine wave current passes through the filter capacitor. The waveform as shown in Figure.3.6. is used for analysis. Hence filter capacitor can be found out as

\[ C_f \frac{dV_o}{dt} = i(t) \implies \Delta V_o = \frac{1}{C_f} \times \int_{T_o}^{T_1} i(t).dt \]  

\[ \implies C_f = \frac{\int_{T_o}^{T_1} i(t).dt}{10V} = 33nF \]  

This is designed as two capacitors of 27nF rated at 2kV (high frequency/ceramic/SMD) in parallel as shown in Figure.3.5. Two high frequency capacitors of 30\(\mu\)F are kept in series across the input power supply to the converter. They are necessary for proper operation at high frequency of 200kHz. They also facilitate taking out dc bus midpoint which would be used in a later section.

### 3.1.6 Design of Snubbers

The snubber capacitors should be designed in such a way that it is high enough to keep the turn off loss to a low value as well as low enough to ensure that they get charged to dc bus voltage (\(V_{dc}\)) in the delay time(\(t_d\)). Delay time(\(t_d\)) is software provided delay between turning on of the complementary switches. This is needed to ensure that dc bus does not get shorted at any point of time. It can be seen that both the leading and lagging leg switches turn off with a very large positive current through it. Hence the use of snubbers are necessary. They can be designed using the procedure followed in [1]. Maximum leading leg turn on current is

\[ I_{leadmax} = 15.3A \]  

\[ C_{lead} = \frac{I_{leadmax} \times t_f}{2 \times V_{dc}} = 6.8nF \]  

where \(t_f\) is the turn off time of IRF540 = 40ns. Minimum leading leg turn off current is

\[ I_{leadmin} = 2.455A \]  

Hence minimum delay time required for complementary switching is

\[ T_D = \frac{2 \times V_{dc} \times C_{lead}}{I_{leadmin}} = 300ns \]  

Similarly maximum lagging leg turn off current is

\[ I_{lagmax} = 9.882A \]  

As observed under Mode2 operation, lagging leg has positive turn on current or negative turn off current for the complementary switch. Hence maximum negative turn off current for the lagging leg switch is

\[ I_{lagnegmax} = 1.2752A \]
\[ C_{lag} = I_{lag_{max}} + I_{lag_{neg_{max}}} \times \frac{T_D}{T_D - t_f} \times t_f = 5.7nF \quad (3.27) \]

The analysis assumes that the current remains constant or changes negligibly during the delay period during transition. Ceramic SMD high frequency capacitors were used as snubber capacitors.

### 3.2 Overall Efficiency

The converter has an efficiency of 89.20\% at maximum load theoretically. The separation of various losses are as shown in Table.3.2, at full load.

<table>
<thead>
<tr>
<th>Type and Device</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leading leg conduction loss (IRF540)</td>
<td>3.8W/device</td>
</tr>
<tr>
<td>Lagging leg conduction loss (IRF540)</td>
<td>3.2W/device</td>
</tr>
<tr>
<td>Leading leg switching losses</td>
<td>0.502W/device</td>
</tr>
<tr>
<td>Lagging leg switching losses</td>
<td>0.609W</td>
</tr>
<tr>
<td>Resonant Inductor: Copper Loss</td>
<td>0.2W</td>
</tr>
<tr>
<td>Resonant Inductor: Core loss</td>
<td>11W</td>
</tr>
<tr>
<td>Resonant Capacitor total losses</td>
<td>Negligible losses</td>
</tr>
<tr>
<td>Transformer Core loss</td>
<td>1.45W</td>
</tr>
<tr>
<td>Transformer: Copper loss</td>
<td>0.04W</td>
</tr>
<tr>
<td>Total losses in rectifier diodes</td>
<td>2.9W</td>
</tr>
<tr>
<td>Total losses in all filter capacitors</td>
<td>100mW</td>
</tr>
<tr>
<td>Total efficiency at full load</td>
<td>89.20%</td>
</tr>
</tbody>
</table>

Table 3.2: Losses in the Converter

The practical efficiency is measured and tabulated in the next section and a comparison is made between theoretical calculations and practical results.
3.3 Open Loop Experimental Results

The converter was operated at scaled down voltage such that operating conditions remain the same. The input voltage fed into the converter was $V_g = 25V$. This voltage was generated using a step-down transformer and rectifier with C-filter as will be discussed in the next chapter. The minimum recognisable pulse width which could be provided using the designed hardware was 0.05. This can be observed in Figure.3.8. The corresponding gate signals given to the switches $S_1$ and $S_4$ are as shown in Figure.3.7.

Similarly, the gate pulses and the quasi square wave for maximum pulse width is as shown in Figure.3.9. and 3.10. respectively. The maximum pulse width is clamped to 0.88 in the program for protection aspects.

When the converter was operated at reduced scale at full load, the waveforms obtained are as shown. The load resistance was $4.1k\Omega$. Figure.3.11 shows the quasi square wave $V_{inv}$. Figure.3.12. shows the tank current waveform in Mode1 operation. Figure.3.13. shows the voltage across the resonant capacitor $V_{cr}$. Figure.3.14. shows the transformer secondary voltage while Figure.3.15. shows the output voltage.
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Figure 3.11: Quasi-Square wave $V_{inv}$

Figure 3.12: Tank Current

Figure 3.13: Tank Capacitor Voltage

Figure 3.14: Transformer Secondary waveform

Figure 3.15: Output Voltage
As discussed earlier, the converter operates in Mode1 as shown for load resistance of 4kΩ which is 100% load as shown in Figure 3.16. As the load is brought below 60%, the converter shifts to Mode2. Figure 3.17 shows the Mode2 operation of the converter. Again if the load is further reduced to below 10%, the converter moves to Mode3 operation.

![Figure 3.16: Mode 1 Waveform](image1)

![Figure 3.17: Mode 2 Waveform](image2)

The efficiency of the converter was measured at a lower operating condition and is compared with the theoretical efficiency. The input voltage supplied was 15V and pulse width was 0.8. The data is as shown in Table 3.3.

<table>
<thead>
<tr>
<th>$R_L$ (kΩ)</th>
<th>$V_{omeas}$ (V)</th>
<th>$I_{inmeas}$ (A)</th>
<th>$\eta_{meas}$</th>
<th>$\eta_{calc}$</th>
<th>$V_{localc}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>552</td>
<td>0.630</td>
<td>64.48%</td>
<td>541</td>
<td>76%</td>
</tr>
<tr>
<td>25</td>
<td>502</td>
<td>0.930</td>
<td>73.99%</td>
<td>508.8</td>
<td>81%</td>
</tr>
<tr>
<td>12.5</td>
<td>440</td>
<td>1.376</td>
<td>78.5%</td>
<td>472</td>
<td>82%</td>
</tr>
<tr>
<td>8.33</td>
<td>412</td>
<td>1.586</td>
<td>80.65%</td>
<td>412</td>
<td>82.7%</td>
</tr>
<tr>
<td>6.25</td>
<td>383</td>
<td>1.938</td>
<td>81.67%</td>
<td>375</td>
<td>83.2%</td>
</tr>
<tr>
<td>5</td>
<td>364</td>
<td>2.098</td>
<td>82.20%</td>
<td>345</td>
<td>83.8%</td>
</tr>
<tr>
<td>4.33</td>
<td>336</td>
<td>2.326</td>
<td>80.88%</td>
<td>321</td>
<td>84%</td>
</tr>
</tbody>
</table>

Table 3.3: Efficiency Measurement and Comparison

The finite value of the parasitic capacitance $C_p$ creates a slight boost in the voltage. This capacitance has to be charged to $V_o$ before the diodes get turned on. This period of no power transfer to the output load, creates a boost in the voltage. The efficiency measured is slightly less than the theoretically calculated efficiency.

The open loop step response of the converter was captured utilising the shutdown facility provided in the driver. The step response of the converter at three different loads
are as shown in the figures below. Figure 3.20 below shows the simulated step response from PSIM. These results are used to model the converter in the next section.

![Figure 3.18: Step Response at Full load](image1)

![Figure 3.19: Step Response at Minimum Load](image2)

![Figure 3.20: Step Response at 25k Load](image3)

![Figure 3.21: Step Response in Simulations](image4)

The settling times are similar to that obtained through simulations. There is slight overshoot in simulated step response at full load which is not clearly visible in the measured step response.

### 3.4 Modeling of the Converter

The averaged state space modeling of the converter is extremely difficult owing to the complex state equations and high degree of non-linearities involved. In averaged modeling, a weighted average of the state equations (weighed by its duration) is taken which is simplified to obtain useful results. In the specific case of an SRC, such simplification is not possible within the scope of this project.

Here, the small signal model of the converter at the extreme points are found out by adding a small sinusoidal disturbance over a frequency range and measuring the magnitude of that frequency component in the output. This was done for a particular extreme operating condition at 12 discrete frequencies to obtain the bode response of the converter at that particular operating condition. Similar bode responses were obtained at other three extreme conditions. These extreme conditions being
• Maximum duty ratio (0.88) and maximum load ($4k\Omega$).
• Maximum duty ratio (0.88) and minimum load ($50k\Omega$).
• Minimum duty ratio (0.1) and maximum load ($4k\Omega$).
• Minimum duty ratio (0.1) and minimum load ($50k\Omega$).

The obtained bode response is as shown in Figure.3.22.

![Bode response of Converter at Extreme Conditions](image)

It can be observed that for the minimum duty ratio-minimum load condition, the converter has an extremely slow pole (relative). For this case, the bode response begins to slope down initially at 20dB/decade and later at 40dB/decade. It can be observed that the two poles are separated by a considerable distance in this case. While in all other cases, the two poles are comparatively close to one another. From the responses it is clear that the converter can best be modelled as a second order system.

The large signal model of the converter was obtained from the step response waveforms in Figures 3.18,19,20,21. This also confirmed the presence of an extremely slow pole at minimum load and low duty ratio. This transfer function was found to be in between the extreme small signal transfer functions.

Three bounding transfer functions were found out to bound all the operating conditions of the converter. It was also verified that for intermediate operating points, the bode response falls between these three binding transfer functions. These transfer functions are as follows

$$G_1(s) = \frac{4200}{4.825 \times 10^{-9}s^2 + 1.834 \times 10^{-4}s + 1}$$  \hspace{1cm} (3.28)

$$G_2(s) = \frac{450}{9 \times 10^{-9}s^2 + 2.927 \times 10^{-4}s + 1}$$  \hspace{1cm} (3.29)
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\[ G_3(s) = \frac{1.26 \times 10^{10}s + 4.284 \times 10^{13}}{s^3 + 13700s^2 + 3.802 \times 10^7s + 1.02 \times 10^{10}} \quad (3.30) \]

The bode response of these bounding transfer functions are as shown in Figure.3.23.

![Figure 3.23: Bode response of the Bounding Transfer Functions](image)

3.5 Controller Design and Implementation

The closed loop controller should be designed such that

- The closed loop system should be stable and not oscillatory. This can be designed in terms of the phase margin of the overall open loop system (controller+converter and other hardware). Phase margin \( \geq 45^\circ \).

- The system should respond fastly to changes in load, input voltage etc. The open loop zero crossing frequency translates as the bandwidth of the closed loop system. This should be as high as possible permitted by the stability constraint.

- There should not be any steady state error. Hence a proportional controller cannot be used.

The first choice that satisfies all the above constraints is a PI controller. A PI controller was designed such that the bounding transfer functions are stable. This ensures the stability of the power converter under all operating conditions within the design limits. The designed PI controller transfer function is

\[ H_c(s) = 10 \times \frac{1 + \frac{s}{1000}}{s} \quad (3.31) \]
Figure 3.24: Bode Response of Converter and Controller

Figure 3.25: Implementation of Controller as a Block Diagram
The overall bode response of the closed loop system is as shown in Figure.3.24. It has a worst case Phase Margin of 45° and a worst case bandwidth of 1.2kHz.

The converter was implemented in an FPGA. The block diagram of the entire closed loop converter is as shown in Figure 3.25. The output voltage is sensed using an isolated voltage sensor card with step-down ratio of 1:200. This voltage is then fed to the FPGA through the ADC. The ADCs are operated at 100kHz sampling frequency. This is the limit set by the hardware constraint. The ADC used is AD7864 which can be sampled at a maximum frequency of 133kHz. This value is then subtracted from the reference set in the FPGA. The reference set is corresponding to 1kV output voltage which is the ADC code of 5V : 3FF.

The output of the subtractor is the error. The error is fed to the designed PI controller implemented inside FPGA using an internal per unit system. The $K_p$ and $K_i$ values of the implemented PI controller was obtained from the designed controller transfer function ($H_c(s)$). The output of the PI controller is limited between the code corresponding to minimum duty ratio of 0.10 and the code corresponding to the maximum duty ratio of 0.88. This code is fed as one of the input to the Phase shifter block. Phase shifter block also receives a PWM of 200kHz and $D=0.5$. This block shifts this PWM at 200kHz by an amount proportional to the limited output of the PI controller. It output the inputted PWM as $PWM_1$ and the phase shifted PWM as $PWM_2$. These signals are again inverted and fed to the delay block. This block delays the rising edge by 300ns ($T_D$) and outputs the signals. These are fed to the respective switches. The next section presents the results of the simulation and experiments on the closed loop converter.
3.6 Closed Loop Experimental Results

The converter was operated in closed loop operation at the reduced input voltage of 25V which was converted to 500V. A reference of 500V was set inside the FPGA. The load was varied in steps initially and various waveforms such as steady state pulse width (D), tank current (I_r) and the output voltage were noted. The Figures 3.26. and 3.27. represents the steady state pulse width attained at minimum load of 50kΩ and corresponding tank current respectively.

The steady state pulse width and the tank current for an intermediate load of 12.5kΩ is as shown in Figure.3.28. and Figure.3.29.

The approximate boundary between Mode1 and Mode2 observed at 7.2kΩ is shown in Figure.3.30. Figure.3.31. shows the steady state pulse width of approximate 0.76 needed in closed loop at full load of 433kΩ.

The speed of response or the bandwidth of the closed loop system can be practically measured by creating a step change in reference. This was done at maximum and minimum load. The responses of the output voltage to step change in reference is as shown in Figure.3.32. at maximum load and Figure.3.33. at minimum load. The settling time of
the step response is 1.6ms at maximum load and 1.4ms at minimum load. The converter output reaches 63.2% of its value in 900μs under full load and 700μs under minimum load. This is closely in agreement with the designed bandwidth of 1-1.2kHz for the close loop converter.

A step change in load was made from maximum load of 4.33kΩ to minimum load 50kΩ and vice versa at a frequency of 200Hz. The measured waveform is as shown in Figure 3.34. A zoomed in figure is shown as Figure 3.35. where we can measure the maximum overshoot as 130V for a sudden change in load as mentioned. The settling time can be clearly measured as around 1ms from the figure. Even under extreme load changes, the maximum overshoot is 130V and steady state is reached in around 1ms.

The efficiency of the converter was measured under closed loop operation while converting 25V to 500V over the entire load range. These results are presented as Table 3.4.
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Figure 3.34: Load Change Response  

Figure 3.35: Load change Response 2

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{o}$</th>
<th>$R_L$</th>
<th>$I_{inmeas}$</th>
<th>$\eta%$</th>
</tr>
</thead>
<tbody>
<tr>
<td>15V</td>
<td>500V</td>
<td>50k$\Omega$</td>
<td>0.35A</td>
<td>57.14%</td>
</tr>
<tr>
<td>15V</td>
<td>500V</td>
<td>25k$\Omega$</td>
<td>0.582A</td>
<td>68.72%</td>
</tr>
<tr>
<td>15V</td>
<td>500V</td>
<td>12.5k$\Omega$</td>
<td>1.101A</td>
<td>72.66%</td>
</tr>
<tr>
<td>15V</td>
<td>500V</td>
<td>8.33k$\Omega$</td>
<td>1.567A</td>
<td>76.67%</td>
</tr>
<tr>
<td>15V</td>
<td>500V</td>
<td>6.25k$\Omega$</td>
<td>2.003A</td>
<td>79.88%</td>
</tr>
<tr>
<td>15V</td>
<td>500V</td>
<td>5k$\Omega$</td>
<td>2.574A</td>
<td>80.00%</td>
</tr>
<tr>
<td>15V</td>
<td>500V</td>
<td>4.33k$\Omega$</td>
<td>3.103A</td>
<td>80.64%</td>
</tr>
</tbody>
</table>

Table 3.4: Efficiency Measurement in Closed Loop
Chapter 4

Auxiliary Hardware Design

This chapter discusses the auxiliary hardwares which were designed to operate the converter in closed loop. The design of the input power supply which feeds power to the converter at 50V is discussed in the first section. The need for switching the load at frequencies as high as 1kHz and the non availability of conventional rheostats prompted the design of a Load Circuit which consumes upto 250W at 1kV. The design of this load circuit is discussed in the next section. Inorder to feedback the scaled down output voltage (1/200) to the FPGA after isolation, a high voltage high bandwidth sensing card was designed. Section 3 looks into the design of this high voltage high bandwidth voltage sensor. A protection and interlock system is designed in Section 4 to prevent accidental shorting of the dc bus.

The next part of the chapter initially studies the method for ensuring the ZVS range using an auxiliary inductor($L_{aux}$) as explained in [1] and [2]. An improvement of the existing method for making it more efficient is suggested later. This requires additional hardware for sensing the tank current. An auxiliary inductor, a 4 quadrant switch and a driver for this 4 quadrant switch are needed. The design of each of these components are considered in the subsequent section.

4.1 Input Power Supply

The power converter needs an input power supply capable of supplying atleast 250W of power at 50V. This is obtained from the 230V mains power supply using an autotransformer, isolated step-down transformer and a rectifier with capacitive filter.

The schematic of the designed input power supply is as shown in Figure.4.1.

The design of the filter capacitor and diodes can be made knowing the maximum current drawn from the power supply. Based on power balance and calculated 89% efficiency under full load, the input current drawn from the converter can be calculated as

$$I_{in} = \frac{P_{out}}{0.89 \times V_{in}} = \frac{250W}{0.85 \times 50V} = 5.88A \approx 6A \quad (4.1)$$

The high frequency filter capacitor of 15$\mu$F at the input of the converter is assumed to supply all the 200kHz ripple current and the current drawn by the converter is assumed
to be pure dc at 6A. When dc current is being drawn from a filter capacitor with C filter, then the voltage output of the rectifier as shown in Figure 4.2.

The capacitor filter should be designed such that the voltage drop ($\Delta V$) is less than 1V. Hence for this operating condition, the charging interval can be assumed to be extremely small. hence $C_{rf}$ can be designed as

$$C_{rf} \times \frac{dV}{dt} = I_{in} \implies C_{rf} = I_{in} \times \frac{\Delta T}{\Delta V} = 60mF \quad (4.2)$$

Such a high value of capacitance can only be realised using electrolytic capacitors whose performance is poor at very high frequency of 200kHz. But the high frequency ceramic capacitors extremely close to the switches can supply those 200kHz ripple current. $C_{rf}$ was designed using 12 capacitors of 4.7mF/50V in parallel. This configuration was found to be cost efficient. APT2X61D40J were chosen as the rectifier diodes which had sufficient current carrying capacity and could block well more than 50V. The designed board is IISC/SANDEEP RECTIFIER PCB V1.0.

## 4.2 Load Circuit

The load should withstand voltage as high as 1kV and consume power upto 250W. Such loads or rheosats were not available as such. The load resistance should vary from 4kΩ to 50kΩ which is the designed load limits for the converter. Moreover, inorder to simulate
pulsed loads occurring in the X-Ray or radar power supplies, the load has to be switched at frequencies as high as 1kHz. These require development of a new load circuit.

The designed load circuit board used 12 50$k$ resistors in parallel to attain 4$k$. The resistors used were THS50 which can dissipate up to 50W when connected to a large enough heat sink. The dissipation in a single resistor is

$$P_{\text{diss}} = \frac{1000^2}{50k} = 20\text{W}$$

12 such resistors connected in parallel amount to 240W at 1kV which is near the designed upper power limit. IGBTs rated at 1200V were connected in series with the load resistances for switching them at high frequencies. The current through each of these shunt branches are

$$I_{\text{shunt}} = \frac{1kV}{50k} = 20mA$$

Hence low current rated IGBTs can be used for the purpose. The IGBTs used were G03H1202 rated for 1220V and 3A. As long wires may be used to connect the load circuit to the converter, the stray inductances can cause damage to the switch. Hence RCD snubbers were added across each of the switches. Anti-parallel diodes are also connected anti-parallelly with the load to remove any harmful effects of stray inductance in the path. The entire load circuit schematic is as shown in Figure 3.3. The detailed schematic of one leg is as shown in Figure 3.4.

The anti-parallel diodes used were MUR 1100. As the frequency of switching was low and the switching losses were also low without snubbers. There is large flexibility in the design of snubber circuit. RCD snubber was designed as $R=1k\Omega$ and $C=10nF$. The designed board is IISc/Sandeep LOAD CIRCUIT PCB V1.0. An isolated gate drive card was needed for switching the loads.

### 4.2.1 Gate Drive Card for the Load Circuit

The signals for switching on and off the loads are produced using the same FPGA used for control. Hence an isolated gate drive card which converts 5V signals from FPGA to similar 15V pulses is needed. A flyback converter driven by LM555 signals is used to
generate an isolated 15V source. The topology of this flyback converter is similar to that of 10kVA inverter gate drive card.

The change in voltage level and isolation is achieved using an optocoupler IC FD3150. This can be operated even at very high frequencies. Due to large gate charge needed for turn on of the used IGBT, an additional driver is used to drive the gate. The driver used was UCC27524. UCC27524 has two channels and hence a single gate drive board was made to drive two IGBTs. The board was tested prior to its addition into the overall system. This gate drive PCB is IISc/SANDEEP LOAD GATE DRIVE CARD V1.0. The schematic is available in Appendix.C.

4.3 Voltage Sensor

The output voltage of the converter has to be scaled down by a factor of 200 and isolated from the actual output of the converter. This is achieved using the isolated voltage sensor card. The existing voltage sensor card for 10kVA inverter cannot be operated above 500V input voltage. Also, the bandwidth of the existing voltage sensor card was 95kHz which is low. As will be seen in the next section, active ripple cancellation needs a high bandwidth voltage sensor. Hence the bandwidth has to be increased at least by a factor of 2.

An isolated power supply of 15V was generated using the flyback converter schematic in the 10kVA inverter gate drive card and LM7815 regulator. The first stage is resistor divider which scales down 1000V to 2.65V (scale down factor 680:1.8). The isolation amplifier used as first stage is ADum3190 which has 2kV isolation voltage range and a higher bandwidth of 400kHz \[16\]. The set gain of the isolation amplifier is 1.

The next stage is an amplifier using high speed operational amplifier AD811. The gain of this stage is set at 2 in non-inverting configuration. Hence the designed voltage voltage sensor converts 1000V at its input to 5.3V. The designed gain of the voltage sensor \((G_{vs})\) is

\[
G_{vs} = \frac{1.8}{681.8} \times 1 \times 2 = \frac{1}{189.39} = 5.28 \times 10^{-3}
\]  
(4.5)

<table>
<thead>
<tr>
<th>(V_{in}) (volts)</th>
<th>(V_{out}) (volts)</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>15mV</td>
<td>(-)</td>
</tr>
<tr>
<td>10V</td>
<td>72mV</td>
<td>(7.2 \times 10^{-3})</td>
</tr>
<tr>
<td>100V</td>
<td>543mV</td>
<td>(5.43 \times 10^{-3})</td>
</tr>
<tr>
<td>200V</td>
<td>1.09V</td>
<td>(5.45 \times 10^{-3})</td>
</tr>
<tr>
<td>300V</td>
<td>1.62V</td>
<td>(5.40 \times 10^{-3})</td>
</tr>
<tr>
<td>400V</td>
<td>2.17V</td>
<td>(5.42 \times 10^{-3})</td>
</tr>
<tr>
<td>500V</td>
<td>2.68V</td>
<td>(5.36 \times 10^{-3})</td>
</tr>
<tr>
<td>800V</td>
<td>4.31V</td>
<td>(5.39 \times 10^{-3})</td>
</tr>
</tbody>
</table>

Table 4.1: Voltage Sensor Linearity Measurement
The linearity of the voltage sensor was measured practically. The results are as shown in Table.4.1. It can be seen that the sensor is linear and has a little offset (15mV) which can be removed in software if necessary.

The voltage sensor was fed with the open loop step of the converter which the sensor tracked perfectly. Hence, the bandwidth of the voltage sensor is much higher than the open loop converter bandwidth of 10kHz.

\[ BW_{es} >> BW_{conv} = 10kHz \]  (4.6)

The bandwidth of the converter was measured practically. The voltage sensor was excited using various sinusoids of different frequency. The sensor was also excited using a square wave and the settling time was measured. The response of the sensor is as shown in Figure.4.5. Figure.4.6 shows the tracking of sinusoidal waveform at 200kHz.

![Figure 4.5: Step Response](image1)

![Figure 4.6: Sinusoidal response at 200kHz](image2)

From the step response and the phase gain relationship, the bandwidth of the voltage sensor was estimated to be 200kHz. The designed voltage sensor is IISc/Voltage Sensor PCB V1.0.

### 4.4 Protection and Interlock System

A protection system is necessary to prevent any stray turn on of the switches. If the complementary switches of an inverter leg are ON at the same time, then the DC bus gets shorted through the switches damaging the switches and the input power supply. It is observed that during the process of burning code into the FPGA, all the output ports are high. If the converter is powered during this time duration, then the dc bus gets shorted. Hence a protection system external to the FPGA is necessary. A provision can be provided to turn off the pulses externally using a manual push button switch. In the later section, we will see that tank current is being sensed and fed to the FPGA, hence if the sensed current is greater than the maximum designed tank current a shutdown pwm pin(SD) is brought high. This high on the SD pin should shutdown the converter.

The protection and interlock system is designed using logic gates. The aim for the design are
• The complementary switches should never be ON at the same time ($S_1, S_2$ and $S_3, S_4$).
• An external manual push button switch shutting down the entire system.
• A high on SD pin should shut down the entire system.

The designed protection system is as shown in Figure 4.7.

![Protection and Interlock system](image)

Figure 4.7: Protection and Interlock system

$S_1, S_2, S_3, S_4$ represent the PWM pulses outputted by the FPGA. SD is the shutdown signal outputted by the FPGA based on its inner current calculation. SHUTDOWN is the output of the protection system which is fed to the shutdown pin of the gate driver IRS2110. The overall delay in shutting down the entire system in case of overlapping pulses is 500ns. $S_1^*, S_2^*, S_3^*, S_4^*$ are outputs of the protection and interlock system which is fed into the appropriate pins of the gate driver. The system can be manually shutdown by pressing the push button. The above system was implemented on a general purpose PCB using CD4071 (Quad OR gate) and three 74HC08 (Quad AND) gate ICs.

4.5 Efficient ZVS Ensuring Method

A method of improving the converter performance by extending ZVS over the entire converter range was suggested and explained in [1],[2]. In this method, the ZVS is ensured over full range by connecting an auxiliary inductor of pre-designed value between the lagging leg inverter leg midpoint and the DC bus midpoint. The modified topology is as shown in Figure 4.8.

It can be seen that the voltage appearing across the auxiliary inductor is a $(+V_{dc}/2, -V_{dc}/2)$ square wave. Hence the current through the inductor ($I_{aux}$) is a triangular with the zero crossing 90° out of phase. These waveforms is as in Figure 4.9. It can be observed from the figure that at the moment the switch $S_3$ of the lagging inverter leg is switched on, the current through $I_{aux}$ is negative and if the tank current is $I_r$ at this instant then the overall current through the switch $S_3$ is

$$I_{S_3} = I_r + I_{aux}$$  \hspace{1cm} (4.7)
Hence if the tank current is zero at that instant, then the switch current becomes negative and ZVS is restored for the lagging leg switches. The auxiliary inductor can thus be designed such that it is more than the worst case positive turn on current for the lagging leg and thereby ZVS over the entire load range can be achieved. The impedance offered by the dc bus capacitance should be very much lower than the impedance offered by \( L_{\text{aux}} \) at this frequency.

However, keeping the inductor connected at all times is inefficient. At full load, when the converter is already switching in Mode1, the connection of \( L_{\text{aux}} \) drives additional
current through the switches and causes increased losses. This reduces the efficiency of the converter. This drawback can be removed by connecting a 4 quadrant switch in series with the $L_{aux}$. This switch should only be turned on when the converter is operating in Mode2. The mode of the converter can be found out by sensing the tank current and using a predictive algorithm implemented in the FPGA. The modified topology suggested is as shown in Figure.4.10.

![Modified Topolgy with Auxiliary Inductor](image)

Figure 4.11: Modified Topolgy with Auxiliary Inductor

$S_5$ and $S_6$ together acts as a 4 quadrant switch with bi-directional voltage blocking and bi-directional current carrying capacity. The switches are connected in series with an inductor, hence the turn off of the switches should be given special care. The turn on signals for the switches $S_5$ and $S_6$ are given from the FPGA. Hence in software, it is ensured that these switches are turned off, only at the zero crossings of the current. This happens midway into the ON time of switch $S_3$ or $S_4$. The computation of $L_{aux}$ and its design is considered in the next sub-section.

### 4.5.1 ZVS Inductor Design

The value of inductance of $L_{aux}$ depends on the maximum positive turn on current or maximum positive turn off current ($I_{lagnegmax}$) of the lagging leg switches. From the earlier analysis, this was obtained as

$$I_{lagnegmax} = 1.2752\, A$$  \hspace{1cm} (4.8)

$$I_{lagmin} = \frac{2 \times V_{dc} \times 5.6}{200} = 1.866\, A$$  \hspace{1cm} (4.9)

Hence the peak current through $L_{aux}$ ($I_P$) is $1.866A + 1.2752A = 3.1412A$. Hence the inductance value can be calculated as

$$L_{aux} = \frac{V_{dc}/2}{2 \times 2 \times f_s \times I_P} = 10.08\, \mu H$$  \hspace{1cm} (4.10)

The design of this inductor was done based on the conventional method followed in [2]. The peak and rms currents through the inductor are 3.14A and 1.85A respectively. Using the conventional method, the design details are as shown in Table.4.2.
### Table 4.2: ZVS Auxiliary Inductor Design

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area Product calculated</td>
<td>265.22mm²</td>
</tr>
<tr>
<td>Core selected</td>
<td>E20/10/5</td>
</tr>
<tr>
<td>No:of turns</td>
<td>6</td>
</tr>
<tr>
<td>Conductor selected</td>
<td>SWG 32: 21 strands in parallel (7 × 3)</td>
</tr>
<tr>
<td>Maximum flux density</td>
<td>0.19T</td>
</tr>
<tr>
<td>Fill Factor</td>
<td>0.135</td>
</tr>
<tr>
<td>Air gap needed</td>
<td>0.127mm</td>
</tr>
<tr>
<td>Core loss</td>
<td>1.02W</td>
</tr>
</tbody>
</table>

The switches selected were IRFL024 SMD MOSFETs. The main converter PCB was designed to incorporate these modifications.

#### 4.5.2 Current Sensor Design

The tank current is sensed in two ways in the circuit. A resistance of 10mΩ/5W is kept in the resonant path. If a larger resistance is kept in the path, it alters the operating point of the converter. Also the rms value of maximum tank current is 10.8A, if a larger resistance is kept for measurement, there would be high loss in the resistor. Hence the chosen measuring resistance is low enough to ensure that there is minimum power loss and there is no change in the operating point and high enough to measure the current without any noise.

The voltage sensed across the current sense resistance ($R_s$) is then processed using an instrumentation amplifier with adjustable gain. As the processing is happening at high frequency of 200kHz, the op-amp used is high frequency 40MHz operational amplifier AD811. It can be seen that the differential signal is the 200kHz near sinusoidal wave, while the common mode signal is a square wave at 200kHz. The finite CMRR of the instrumentation amplifier distorts the sensed current waveform at the transition points of the square wave. The sampling of the current waveform can be avoided at those points to remove these errors. The sensed current waveform is as shown in Figure.4.11.

![Figure 4.12: Current Sensor Output Waveform](image)

A current transformer was also used to sense the current accurately. The core used was T28. As the current is near sinusoidal, the conventional design procedure for sinusoidal
transformer was done. The turns ratio of 1:12(2:24) was chosen. Hence the RMS value of current in the secondary is

\[
I_{secrms} = \frac{10.8}{12} = 0.9A.
\]  

(4.11)

A burden resistance of 1\(\Omega\) on the secondary produces an rms secondary voltage of 0.9 \(\times\) 1 = 0.9\(V\). The maximum value of flux density in the core can be calculated as

\[
B_m = \frac{V_{sec}}{N_s \times 200 \times 10^3 \times 4.41 \times A_c} = 15mT
\]  

(4.12)

This is well within the limits of the permitted maximum flux density. The current transformer was made and an instrumentation amplifier was used to process the sensed waveform and scale it appropriately. The current waveform can be obtained with minimum distortion using this method.

### 4.5.3 Predictive Algorithm

The sensed current waveform along with other available data such as the pulse width of quasi-square wave \((V_{inv})\) are used to find the mode of operation of the converter. The current waveform which is at 200kHz has to be sampled at much higher frequency to get the maximum data points. However the maximum sampling frequency available is 200kHz, hence the current cannot be sampled even twice every cycle. Moreover the sampling point is synchronised with respect to the gate pulses, cannot be made to sample at the peak or a finite location on the current waveform (assumed sinusoidal) always. This hardware constraint makes it impossible to recreate the current waveform inside the FPGA.

This problem was overpowered using a technique called Interleaved sampling. In this technique, the current waveform is sampled at two different locations at two consecutive cycles. The assumption which is made is

- The operation of the converter is in steady state and the current waveform does not change in two consecutive cycles.
- The predictive algorithm uses steady state sinusoidally approximated equations of the converter to find out the mode of operation and the peak voltage.

The block diagram for implementation of this efficient ZVS scheme is as shown in Figure.4.12.

The inputs to the algorithm developed are

- Sampling instant 1 \((T_1)\) is in the positive half cycle during turn off of the leading leg switch \(S_1\). The sample is \(A_1\).
- Sampling instant 2 \((T_2)\) is in the positive half cycle in the next cycle during the turn on of the lagging leg switch \(S_4\). The sample is \(A_2\).
- The steady state pulse width \((D)\). This can be obtained by interacting with the main pulse generator.
Let the midpoint between the turn on of $S_1$ and $S_4$ or the zero crossing of the fundamental of $V_{inv}$ be defined as $wt = 0$ point. Let $\Theta$ be defined as

$$\Theta = \frac{(1 - D) \times \pi}{2}$$

(4.13)

Then the phase lag of current waveform ($\phi$) can be found out as

$$\Phi = \cot^{-1} \left( \frac{A_2 + A_1/A_2 - A_1}{\tan \Theta} \right)$$

(4.14)

The overall flowchart for the prediction algorithm can be drawn as in Figure 4.13.
\[ \Theta = (1-D) \times \frac{\pi}{2} \left( \frac{A_1 + A_2}{A_2 - A_1} \right) \]

\[ \tan(\Theta) \]

\[ k = \frac{k_1}{\tan(\Theta)} \]

\[ \phi = \text{acot}(k) \]

\[ \Theta + \phi \]

\[ \sin(\Theta + \phi) \]

\[ I = \frac{A_2}{K_2} \]

\[ R = \frac{\pi V_0}{2I} \]

\[ R > R^* \]

\[ \text{Yes} \]

\[ \text{NO} \]

\[ \text{MODE1} \]

\[ \text{MODE2} \]

\[ \text{Figure 4.14: Prediction Algorithm Block Diagram} \]
Chapter 5

Active Ripple Cancellation

As mentioned earlier, the designed SRC is operated under pulsed load conditions. The load is switched between minimum and maximum load at a frequency which can be as high as 1kHz. This is common in X-Ray power supplies used in medical applications as well as in radar power supplies used in defence applications. Under closed loop voltage control operation, such pulsed loading causes ripple in the output voltage. This can seriously corrupt the power supply. An active ripple cancellation technique is suggested in this chapter which helps to completely cancel the ripple due to pulsed loading. The first section explains the method in detail while the second section presents the simulation results of the proposed method. The third section discusses the design of the hardware for implementing this active ripple cancellation technique and final section presents the experimental results.

5.1 Method : Using Linear Regulator of Lower Rating

The active ripple cancellation technique presented here uses a linear regulator of much lower rating to cancel the output voltage ripple. The linear regulator should be rated for a voltage slightly greater than the actual ripple voltage. A negative linear regulator is used and it works on the ground of the output voltage. This method can be extended to even very high voltages of 10 or 20kV inorder to remove ripples of magnitude upto 1kV.

The block diagram for implementing the method is as shown in Figure.5.1.

The simulation results showed that the maximum peak to peak ripple in the output voltage is 80V. Hence the linear regulator was designed to operate on an auxiliary voltage of 100V. This voltage is generated using a flyback converter. It is to be noted that the $V_-$ of the 100V is connected to the ground of the SRC output and $V_+$ of the 100V is considered as ground reference. The ripple in the output voltage is sensed, amplified and added with an offset and fed as a reference to the negative linear regulator. If the bandwidth of the linear regulator is high, it can track the reference and recreate the same ripple at its output. Hence if these two terminals are taken as output of the load, then the output voltage can be obtained as ripple free. Through closed loop action, the ripple is actively cancelled by the linear regulator. The load current passes through the transistor in the regulator and causes considerable loss in the transistor. These are calculated in later section.
It can be seen that the negative voltage regulator operates in stable negative feedback mode. If the voltage at the output of the regulator becomes more negative, then the op-amp output reduces (becomes more negative). This in turn increases the current through the transistor $Q_2$ and makes the voltage at the base of $Q_1$ less negative and thereby reducing the output voltage.

The regulator was properly designed such that proper feedback occurs for voltage output of the regulator in the range -10V to -90V. The designed schematic is available in Appendix.C. The linear regulator output was initially tested assuming sinusoidal ripple at frequencies till 10kHz. This regulator can be used for perfect cancellation of such ripple. However when the output of SRC contains square wave ripple, then the high frequency components cannot be tracked by the regulator and pass through. However in the practical case, the ripple waveform for pulsed loading at $D=0.5$ is as shown in Figure.3.34. The results of cancellation of such a ripple is presented in a later section in this chapter.

### 5.2 Hardware Design

The hardware necessary for the implementation of the suggested active ripple cancellation scheme needs the following hardware.

- A 100V 0.1A isolated power supply which is developed using a flyback converter driven by TL494 driver. The output current needed from this power supply is very low as it needs to supply currents through the shunt branches of the linear regulator only.

- A high bandwidth isolated voltage sensor. The earlier designed voltage sensor of 250kHz bandwidth is used for this purpose also.
• A bandpass filter which has gain 1 and zero phase lag over a range of frequencies from 50Hz to 10kHz. It should attenuate both dc and ripple at 200kHz completely and pick up only the pulsed loading ripple.

• A processing circuitry and offset adder is a circuit involving op-amps for controlling the gain of the sensed voltage ripple. It also adds a negative voltage offset so that the reference set is negative always (only then it can be tracked by the regulator).

• The negative linear voltage regulator which has maximum bandwidth of atleast 1kHz.

The calculated power loss in the regulator ie, in the transistor $Q_1$ was 13.8W. Hence the transistor has to be mounted on a large heat sink. Darlington pair of PNP transistors 2SB150 was used as $Q_1$. These transistors had very high bandwidth which improves the overall bandwidth of the linear regulator. The output capacitor of the linear regulator should be minimum just to ensure the stability of the regulator. The simulations showed that a capacitance of 100pF can stabilise the system and the resultant regulator showed a bandwidth of 10kHz.

The bandpass filter was designed with cut off frequencies at 10Hz and 50kHz. The upper cut-off frequency is not of importance as the bandwidth of the linear regulator is much lesser (10kHz). The schematic of the band-pass filter is as shown in Figure 5.2.

![Figure 5.2: Band Pass Filter Schematic](image)

The designed value of the components were

<table>
<thead>
<tr>
<th>Component on Schematic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>150Ω</td>
</tr>
<tr>
<td>$R_2$</td>
<td>100kΩ</td>
</tr>
<tr>
<td>$C_1$</td>
<td>$1\mu F$</td>
</tr>
<tr>
<td>$C_2$</td>
<td>$2.7nF$</td>
</tr>
</tbody>
</table>

Table 5.1: Band Pass Filter Component Values

These hardware were made into the IISc/Sandeep Regulator PCB V1.0.
5.3 Experimental Results

The first test performed on the hardware was to determine the bandwidth of the Overall Active Ripple Cancellation Circuitry. This was performed by giving sinusoidal signals of various frequencies as input to the band pass filter and noting the gain and phase of the tracked output. The output filter capacitor had to be increased to 66nF to stabilise the linear regulator, hence a decrease in bandwidth is expected. Figure 5.3 shows the output of the linear regulator for a 200Hz reference sinusoidal signal. It is observed that, the output tracks reference with no visible phase lag.

Figure 5.3: Regulator output at 260Hz

Figure 5.4: Regulator output at 1kHz

Figure 5.4 shows the output of linear regulator for 1kHz sinusoidal reference signal. There is very less phase lag of less than 10° observed. Figure 5.5 shows the output of the linear regulator at 2kHz reference sinusoid. It is observed that there is visible phase lag of over 40° as well as a high degree of nonlinearity in the output.

Figure 5.5: Regulator output at 2kHz

The experimental results showed that the overall bandwidth of the Active Ripple Cancellation Circuitry is about 1.3kHz. Hence it can be used for effective ripple cancellation for frequencies up to 1.3kHz. Figure 5.6 shows the voltage when the output of SRC is directly fed to the pulsating loads at 200Hz where the ripple magnitude is almost 50V. Figure 5.7 shows the output voltage when the load is pulsating and the designed active ripple cancellation strategy is employed. It can be seen that the ripple gets cancelled to almost 8V i.e., the ripple gets cancelled by more than 80%. With further fine tuning of the system, more than 95% ripple cancellation can be achieved.
CHAPTER 5. ACTIVE RIPPLE CANCELLATION

Figure 5.6: SRC output

Figure 5.7: Active Ripple cancelled output
Chapter 6

Conclusion

6.1 Scope of Future Work

- The active ripple cancellation scheme employed linear regulator to cancel out the pulsed loading ripple. The bandwidth of the linear regulator turned out to be much lesser than expected. Still ripple cancellation in the range of 80% to 90% could be achieved even with a low bandwidth regulator of 1.3kHz bandwidth. The magnitude and frequency components in the ripple can be decreased by artificially slowing down the converter. The output capacitor at 1KV can be increased and thereby reducing the open loop bandwidth of the system. This also reduces the closed loop bandwidth of the system and makes the response slower. The high frequency components will be much lower in that case which the regulator can easily track. However when operated at in open loop then a faster converter is preferred.

- The active ripple cancellation technique can be employed using a switched mode power converter instead of regulator. Through proper topology selection and proper controller design, SMPCs with closed loop bandwidth in the range of 1kHz to 10kHz can be made. The reference to the closed loop controller is given in a similar way by sensing the output voltage and passing through band pass filter and offset adder. These have an added advantage of much higher efficiency compared to linear regulator based active ripple cancellation.

- If a higher input voltage is available, then SRC can be operated at a higher frequency factor and a Q factor to attain the same output voltage. Under such conditions, the advantages of soft switching can be easily attained. A higher frequency factor although reduces the gain and increases the value of resonant components, a lower current rating can result in reduced size of the resonant tank.

6.2 Remarks

- The first objective of the project was to develop a model for X-Ray and radar power supplies at a lower power and voltage level and to stabilise the model in closed loop with a speedy response. The hardware built towards this consists of

  1. The power converter SRC board with provision for the efficient ZVS ensuring method discussed in the report. IISc/ Sandeep Warrier Resonant Converter PCB V1.0.
2. A high bandwidth voltage sensor of 250kHz estimated bandwidth. Voltage Sensor PCB V1.0.

3. Two channel isolated gate drive cards for switching till 100kHz. IISc/ Sandeep Load Gate Drive Card V1.0.

4. Two sets of instrumentation amplifier for current sensor output processing. IISc/ Sandeep Current Sensor PCB V1.0.

5. The load circuit with resistance variable from 4kΩ to 50kΩ at 1kV. IISc/ Sandeep Load Circuit PCB V1.0.

- The active ripple cancellation scheme was tested on the closed loop stabilised SRC for pulsed loading. The hardware designed and built for implementing the active ripple cancellation scheme is IISc/ Sandeep/ Regulator PCB V1.0.

- The experimental results in open loop and closed loop matched the theoretical and simulated gain of the converter. A small increase in gain observed may be due to finite parasitic capacitance of the step up transformer. The open loop and closed loop bandwidth of the converter measured experimentally were also in close agreement with the theoretically designed and observed bandwidth through simulations.

- The range of different modes of operation measured experimentally varied slightly with the analysis results. These can be due to the experimental errors in measuring a high frequency (200kHz), low magnitude signal. The ZVS ensuring method is efficient in helping the converter attain ZVS over the entire load range.

- However in active ripple cancellation, the simulated and experimental bandwidth of the linear regulator varied by a large extent. This may be due to non ideal op-amps having finite bandwidth, the finite bandwidth of the transistors used etc. Better methods of improving the efficiency and better ripple cancellation are suggested in the previous section.
Appendix A

Expressions for Mode 2 and Mode 3 of SRC
Appendix B

Code for Converter Solutions
Appendix C

Schematics of the Designed Boards